

GA-M68SM-S2

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	PROCESSOR HT INTERFACE
05	PROCESSOR DDR2 INTERFACE
06	PROCESSOR CONTROL & DEBUG
07	PROCESSOR Power & Gnd
08	DIMM 1,2
09	DIMM 3,4
10	DIMM TERMINATION
11	MCP61-CPU
12	MCP61-PCIE
13	MCP61-DAC, RGMII
14	MCP61-PCI
15	MCP61-SATA, IDE
16	MCP61-USB, HD-Audio, GPIO
17	MCP61-Power, Gnd
18	PCI EXPRESS x16, x1 SLOT
19	PCI 1,2,SLOT
20	ITE 8716GB/CX, SPI BIOS.
21	Realtek 8211BL GIGA LAN
22	H/W MONITOR & FAN CONTROL
23	IDE/FDD/COM/LPT
24	F_USB/ R_USB
25	ALC888 HD-AUDIO

SHEET TITLE

Revision:1.0

26	AUDIO JACK, L_OUT, F_AUDIO
27	FRONT PANEL POWER SEQUENCE
28	ATX POWER CONN
29	PWM ISL6312
30	VCC12_DUAL,VCC12_HT,VDDA25 POWER
31	DDRII POWER
32	TI TSB43AB23 1394

Component value change history

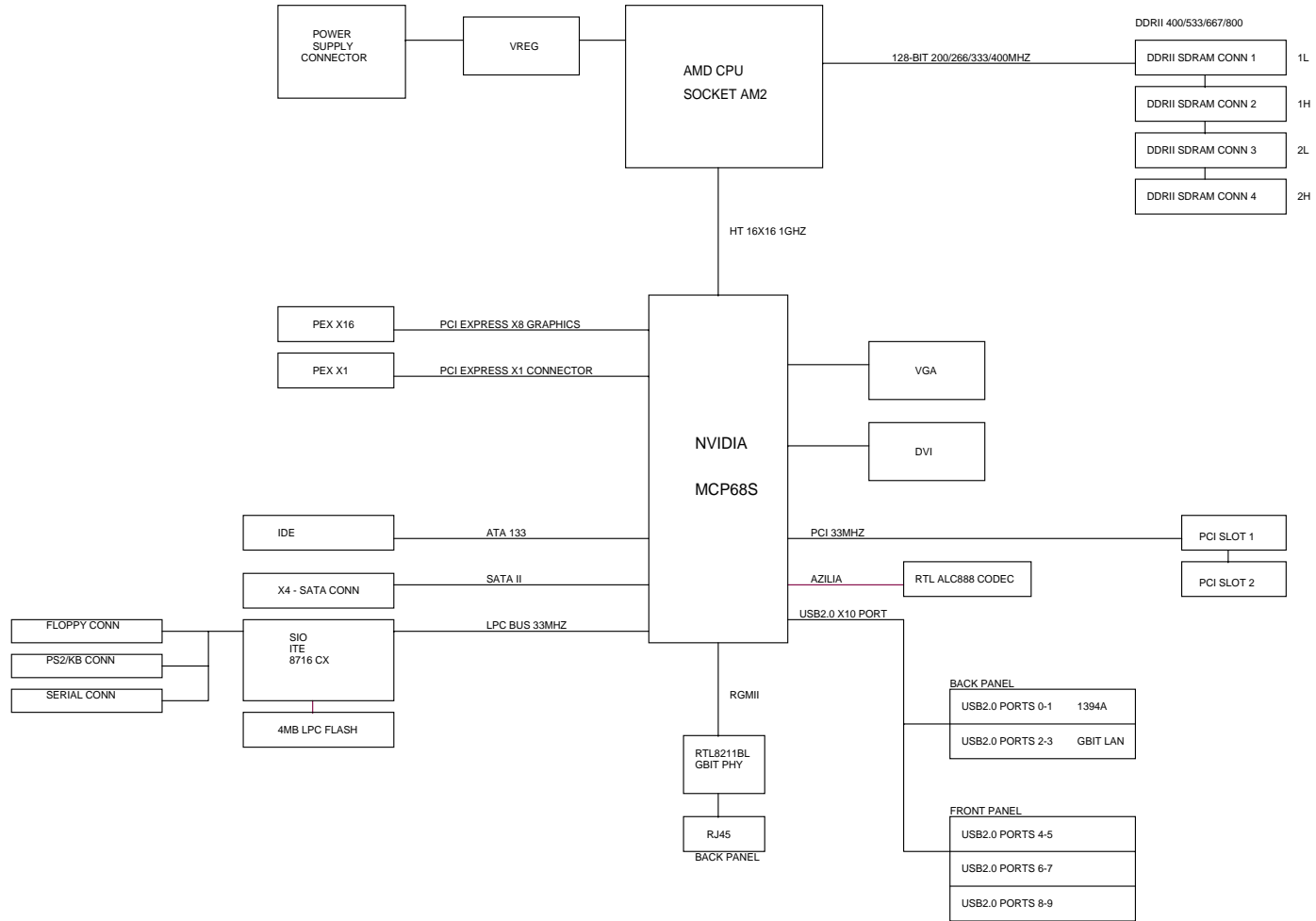
P-Code: A95096-0

Date	Change Item	Reason
2007.01.30	0.1 E_BOM release PCB:0.1	New BOM release A1 Bug: need to push Power Button for 10 seconds to boot up Change KB/MS source. Change F_USB fuse. Change CD1 . USB BIAS CHANGE TO 1.1K (R99)
2007.03.27	0.2 E_BOM release PCB:0.2	Change spec. add LPT port, and remove AM2+ dual plan support.
2007.04.16	0.3 D_BOM release PCB:0.3	
2007.06.22	1.0A D_BOM release PCB:1.0	HDMI ROM CLK/DATA change for Nvidia comments. Fix LED don't light without CPU Change DVI footprint Change 1394 to grey. 1394 EEPROM free 74HCT32 back Add HDCP ROM (I2C and CHIP) ADD R437 300 ohm (add 5Vsb Loading for PSU issue) C1065 add 1M res to GND [NV AP NOTE Request]
2007.07.11	1.0B P_BOM release PCB:1.0	DC5 --> 220P & DR12 --> 5.1K for Choke noises LC4,LC5,LC6 -->10P & PCN1,PCN2,PCN3,PCN4 ADD 180P EMI Request Remove PCB (祥豐) ADD Packing BOM
2007.07.11	1.0C P_BOM release PCB:1.0	ADD R & C & DVI CONN Second source Change 1394+usb CONN 30u ----> goldflash

Circuit or PCB layout change for next version

Date	Change Item	Reason
2007.01.29	0.1 Gerber Out	CPU: VDD=VCORE, CPU_VDDNB=VCORE_NB, VTT=DDRVT VSS=GND
2007.03.26	0.2 Gerber Out	PWM support AM2+. ISL 6323
2007.04.13	0.3 Gerber Out	PWM change back to ISL6312, add LPT port
2007.06.21	1.0 Gerber Out	Adjust PSU Power issue ADD HDCP EEPROM circuit

BLOCK DIAGRAM



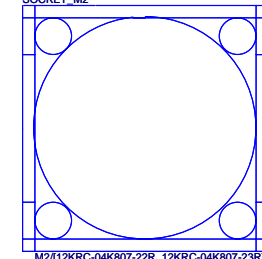
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L0_CADIN_H[0..15] <L0_CADIN_H[0..15] <11>
L0_CLKIN_L[0..1] <L0_CLKIN_L[0..1] <11>
L0_CLKIN_H[0..1] <L0_CLKIN_H[0..1] <11>
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] <11>
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] <11>
L0_CLKOUT_L[0..1] <L0_CLKOUT_L[0..1] <11>
L0_CLKOUT_H[0..1] <L0_CLKOUT_H[0..1] <11>



CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

SOCKET_M2

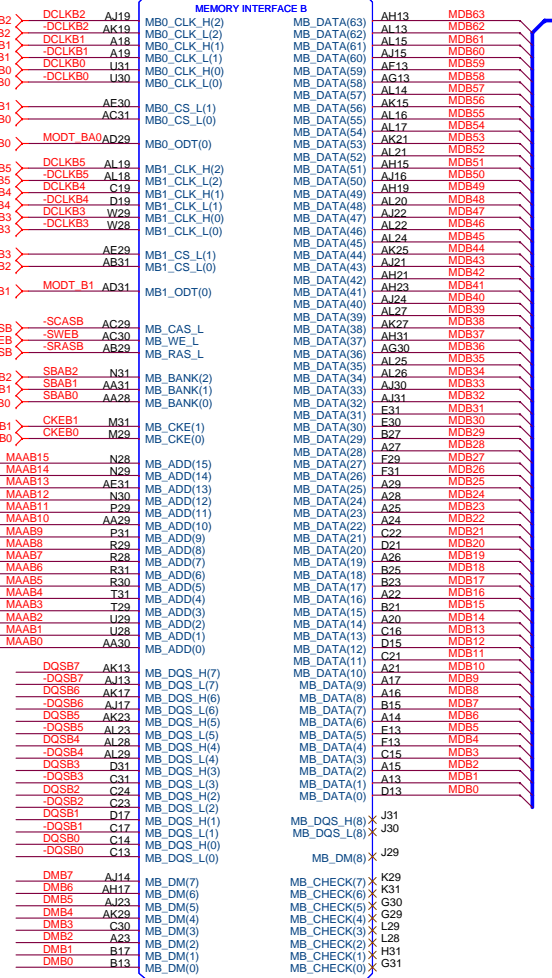
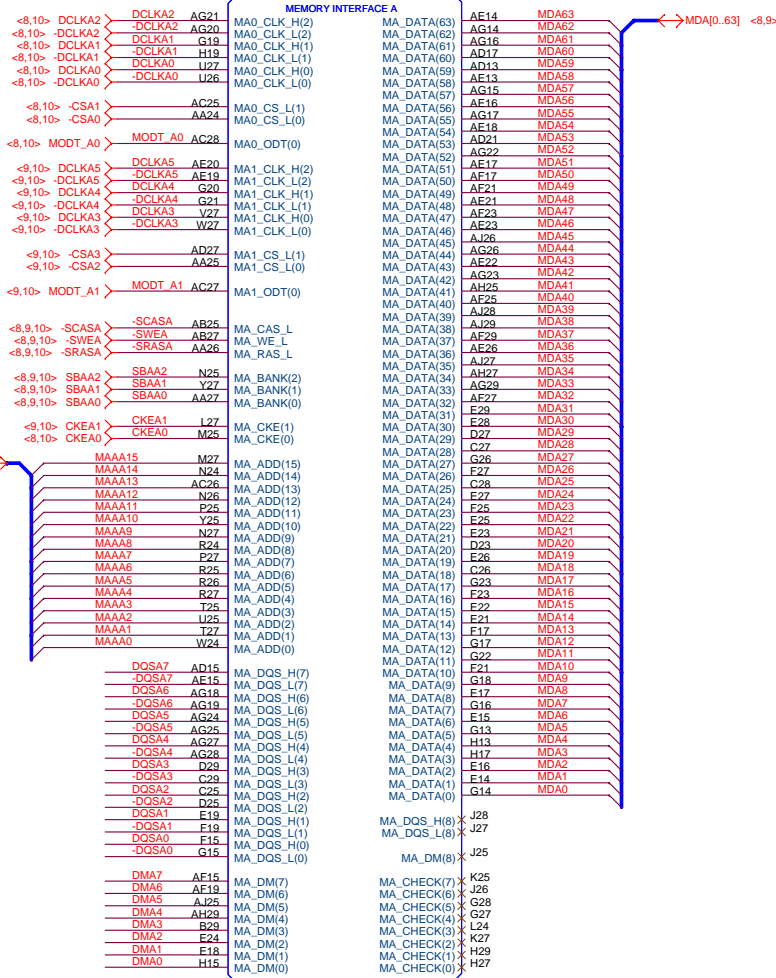


M2CPUC

M2CPUC

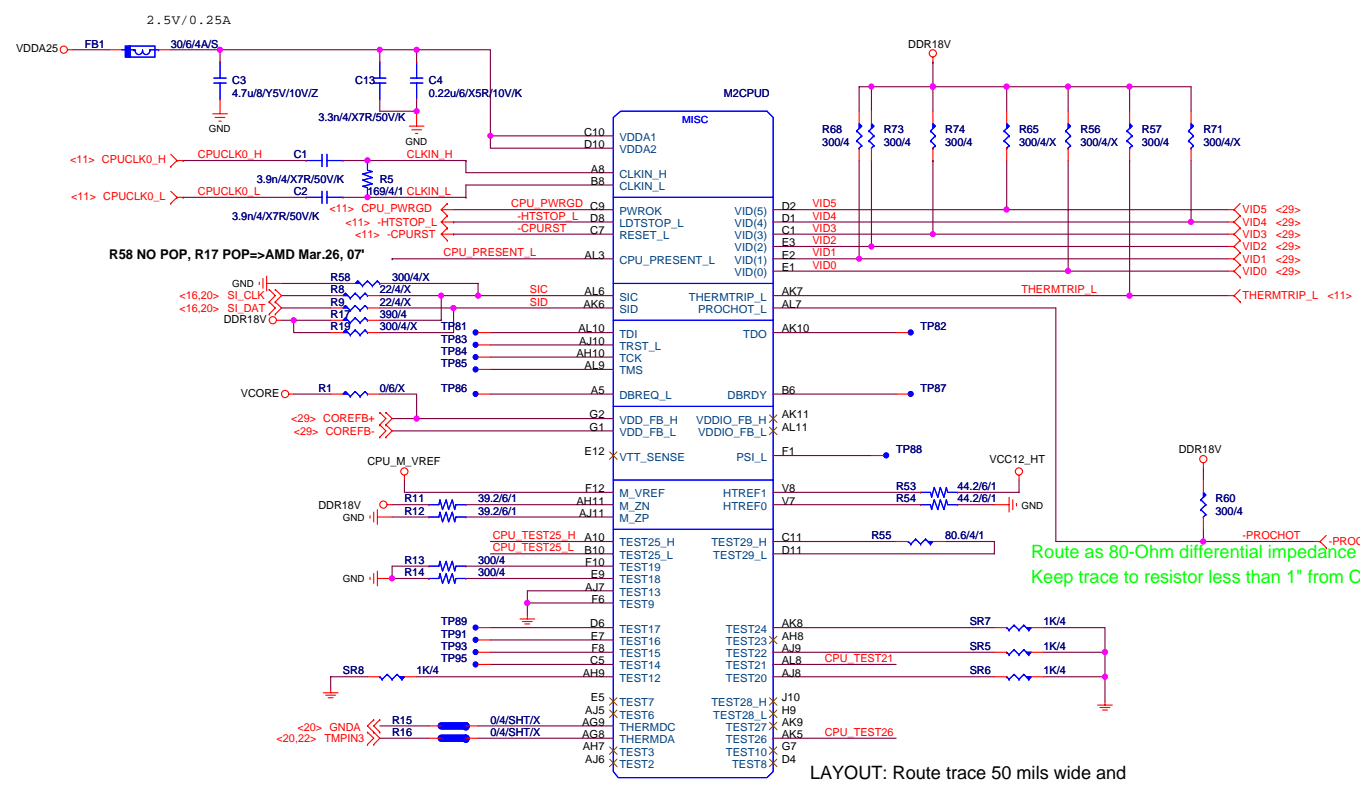
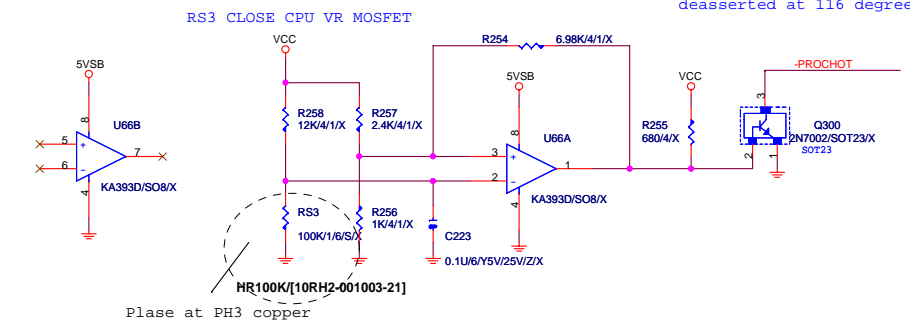
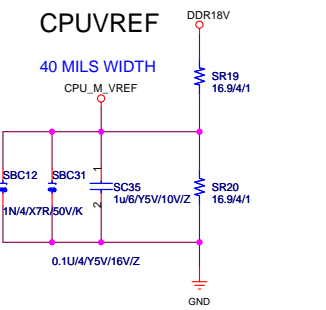
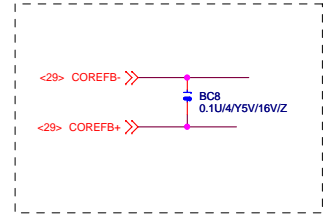
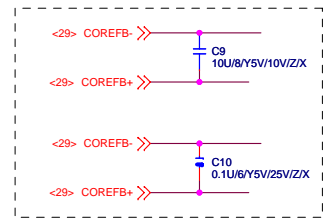
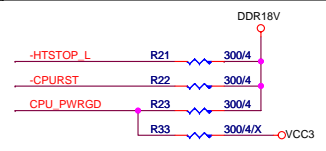
MEMORY INTERFACE A

MEMORY INTERFACE B



GIGABYTE

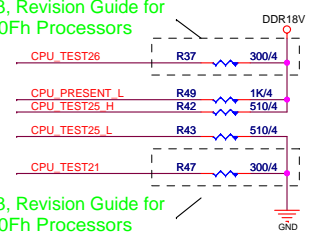
CPU DDRII MEMORY		
Title		
Size	Document Number	Rev
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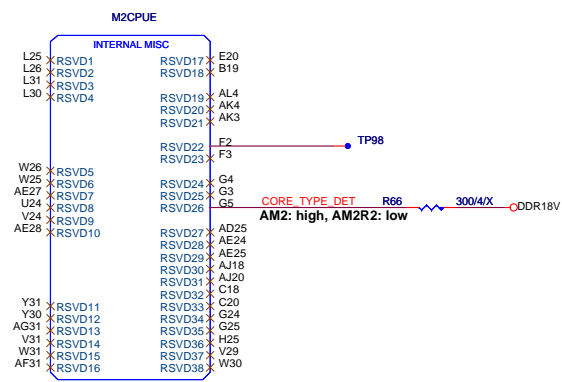
Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin

LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.

Erratum 133, Revision Guide for AMD NPT 0Fh Processors

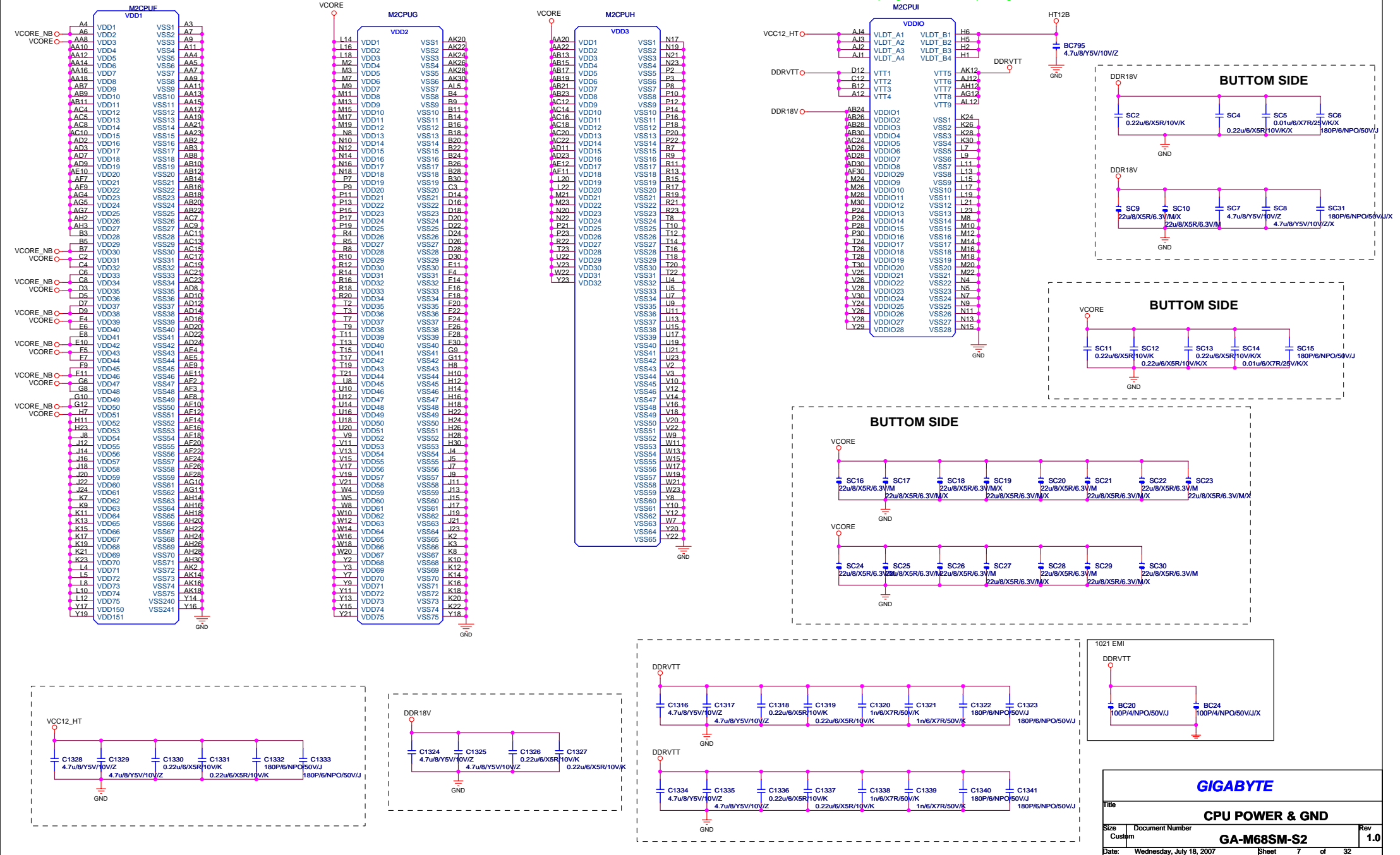


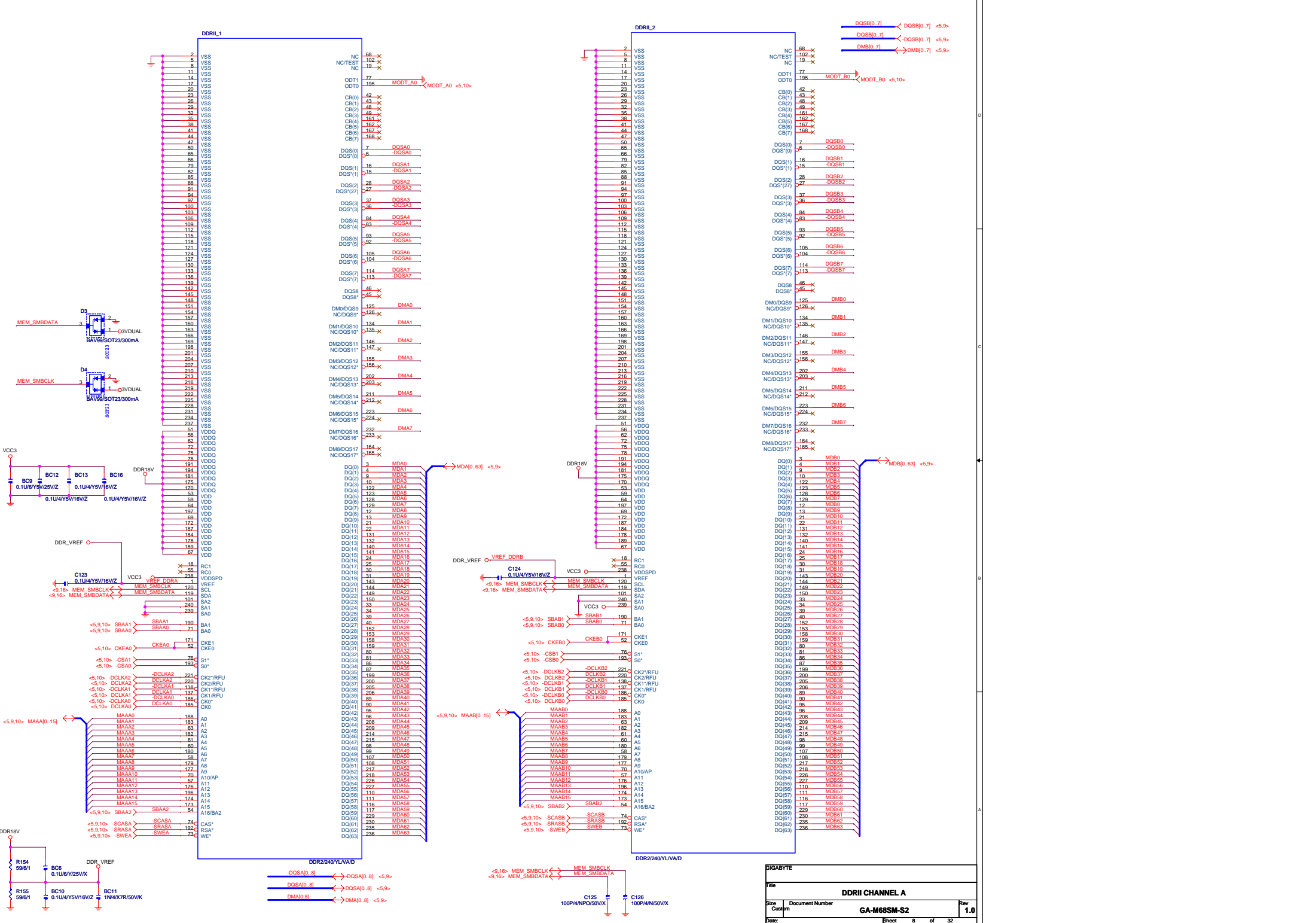
Erratum 133, Revision Guide for AMD NPT 0Fh Processors



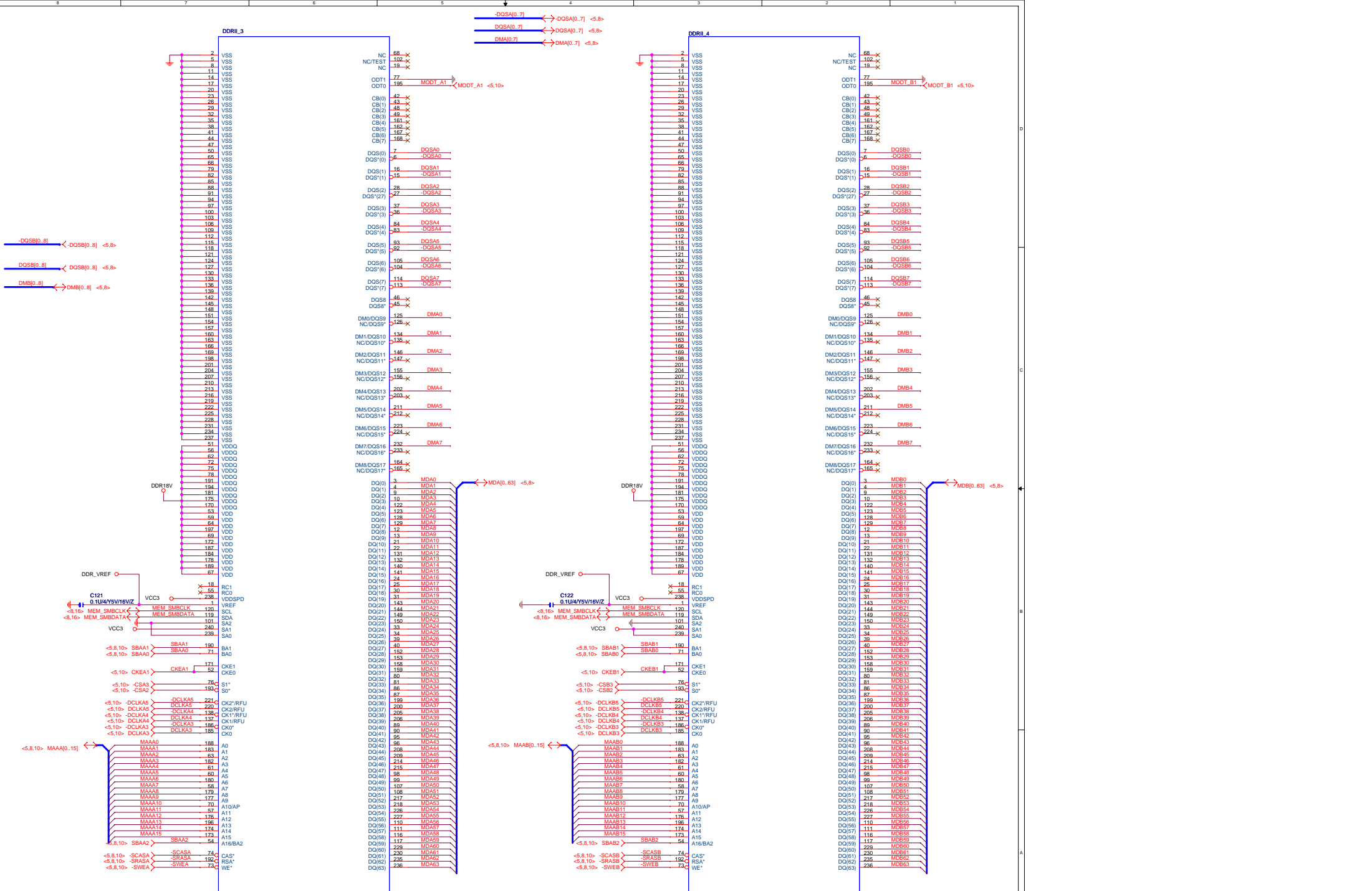
GIGABYTE		
CPU CONTROL		
Title	CPU CONTROL	
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VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

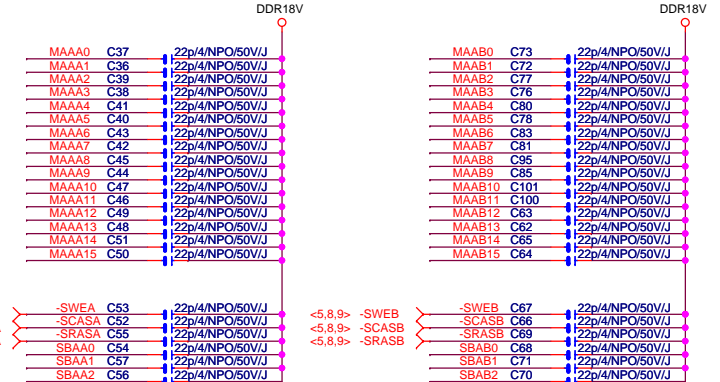
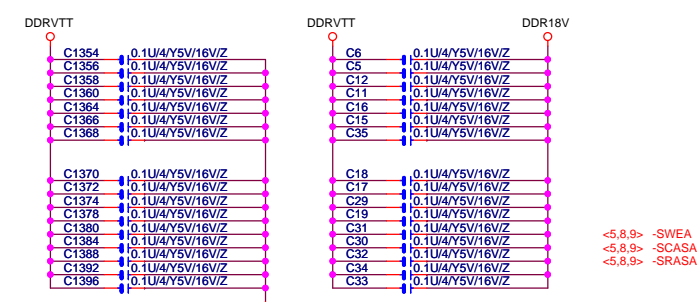
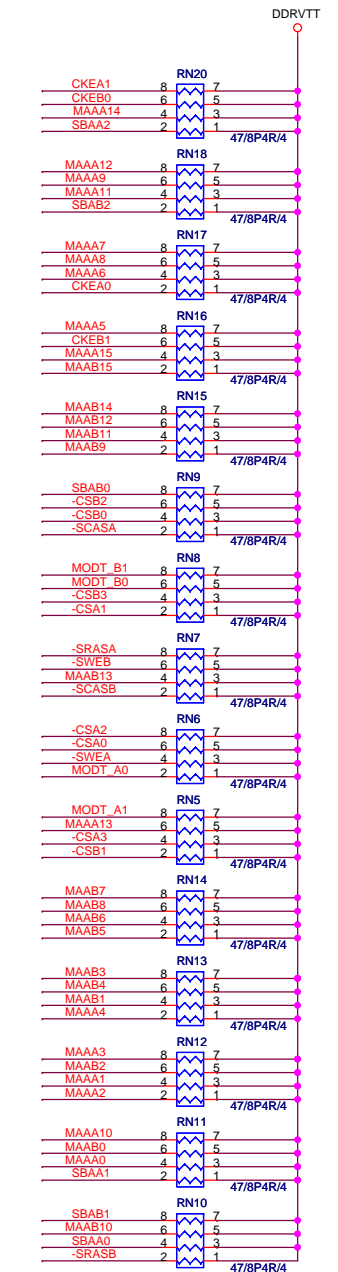
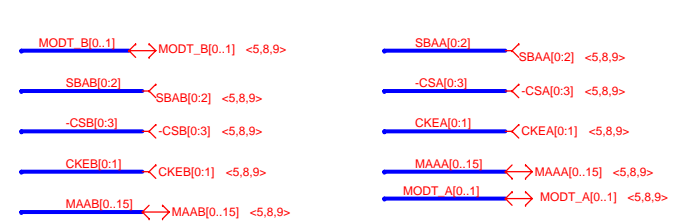
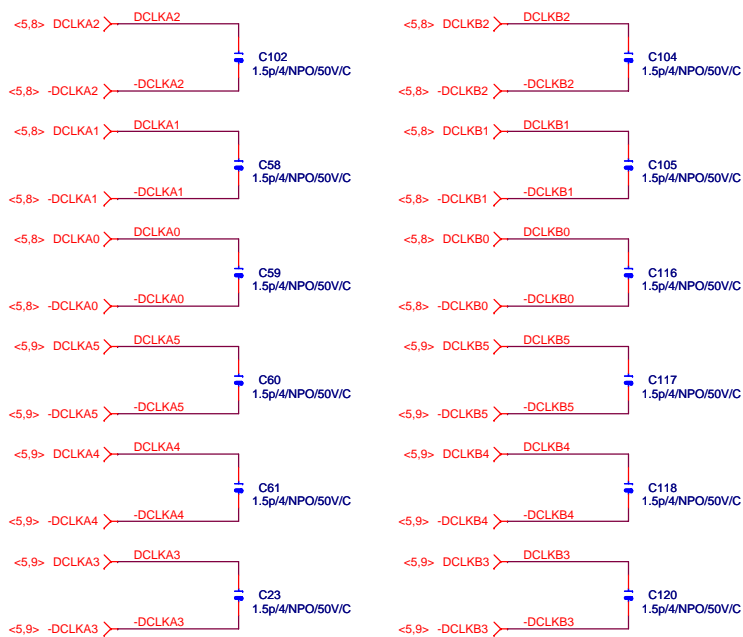


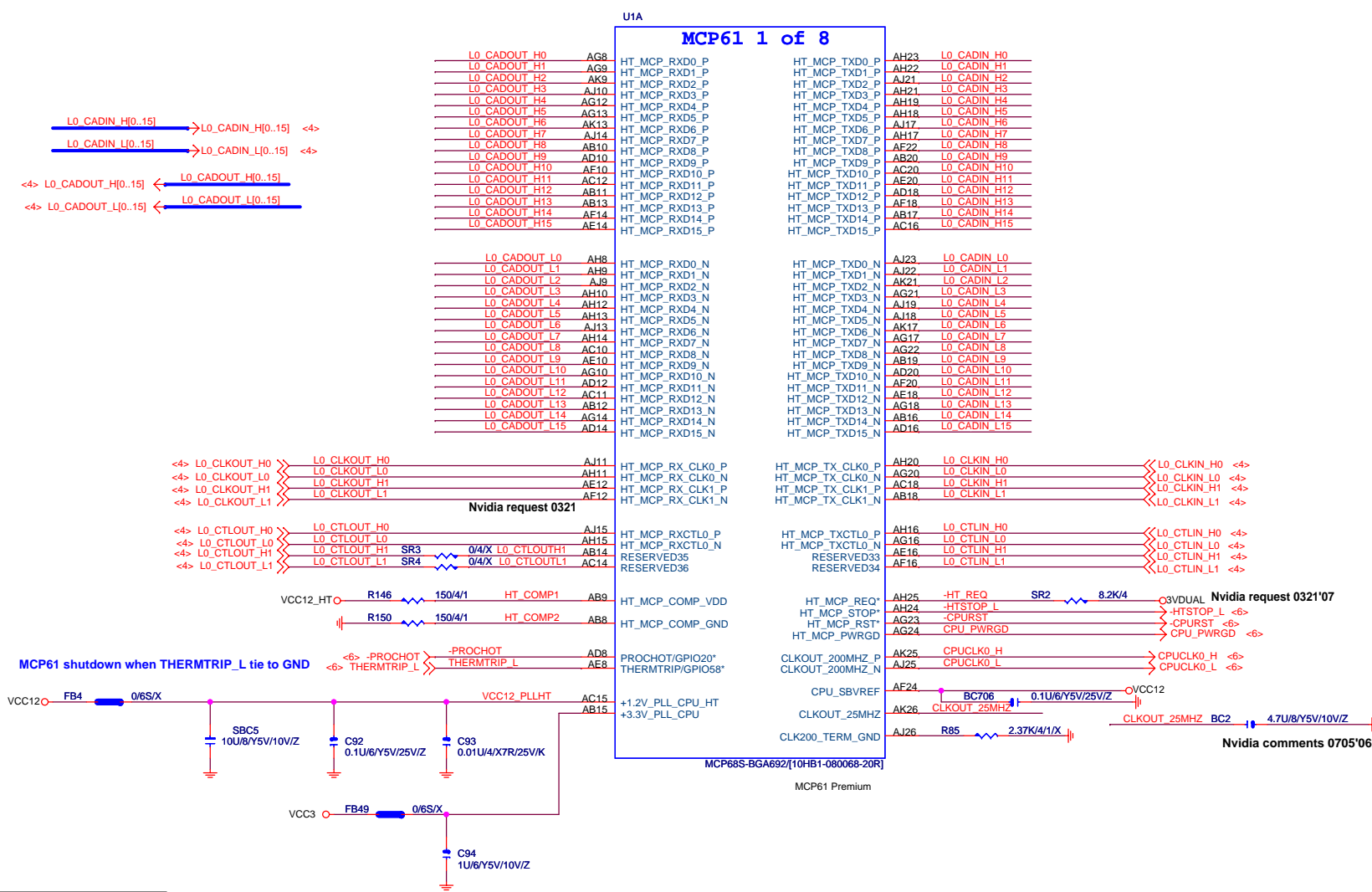


8GBYTE
 DRRI CHANNEL A
 Size Custom
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 Date: 8 of 32
 Rev 1.0

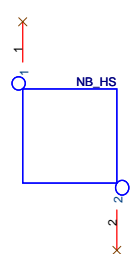


8iGBYTE	
File	DDR1 CHANNEL B
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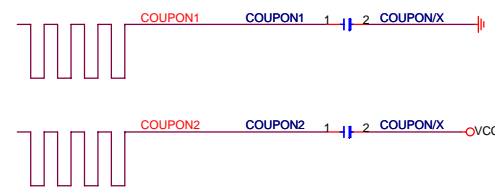




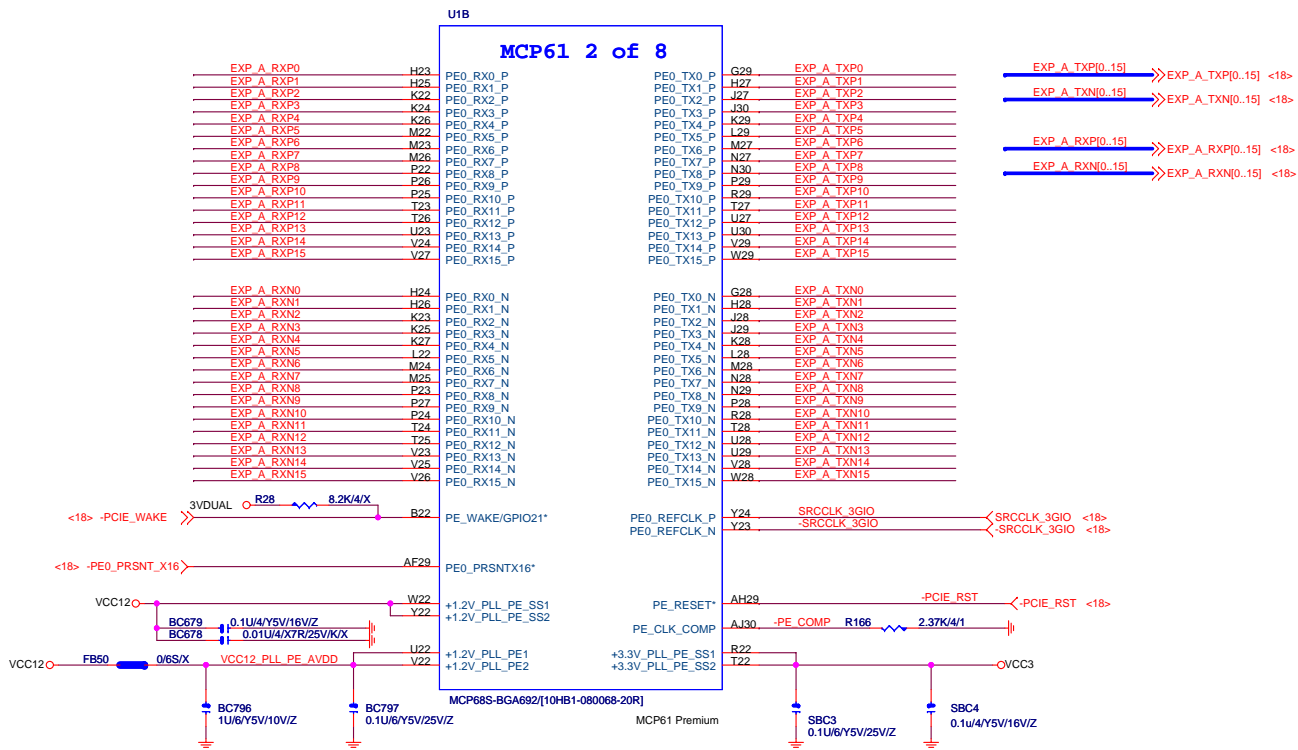
N.B HEATSINK



BGASINK_NB[12SP2-01A002-52R_12SP2-01A002-53R_12SP2-01A002-52R]



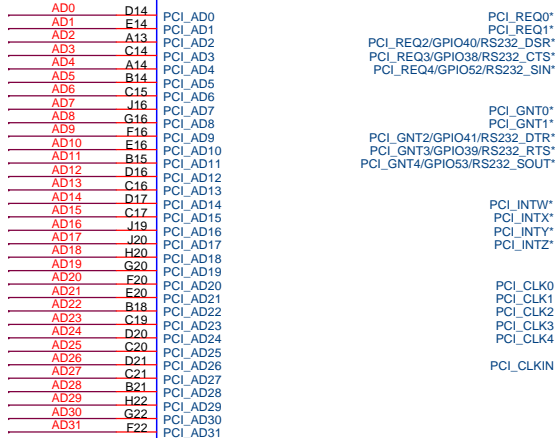
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Title			
C51-HOST			
Size Custom	Document Number	GA-M68SM-S2	
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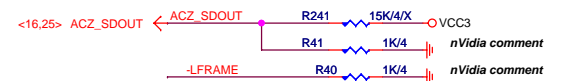
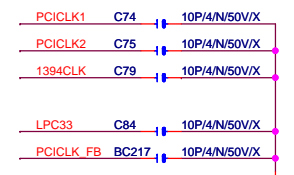
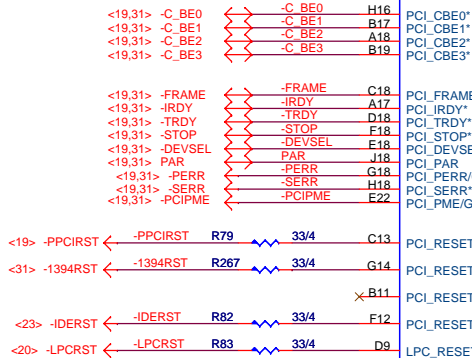
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U1D

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MCP68S-BGA692(10HB1-080068-20R)



BIOS STRAP:

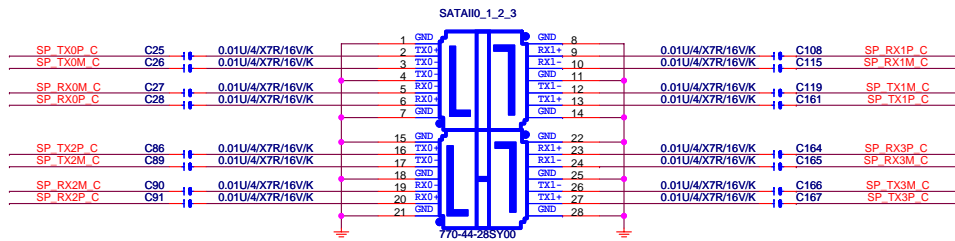
ACZ_SDOUT
-LFRAME

0 0 = LPC BIOS
0 1 = PCI BIOS
1 0 = SPI BIOS (Default)
1 1 = RESERVED

0.1 use LPC BIOS, 0.2 change to SPI BIOS

GIGABYTE

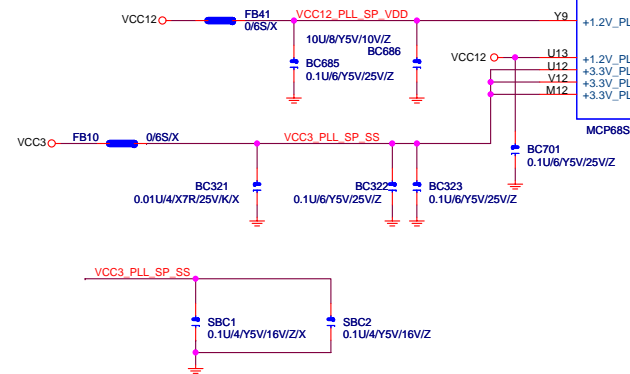
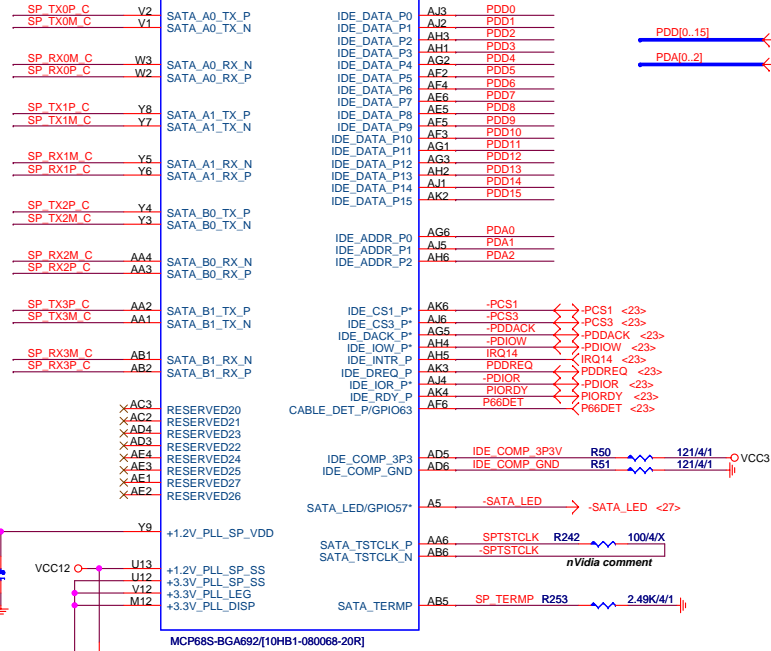
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Size Custom	Document Number	Rev
	GA-M68SM-S2	1.0
Date:	Wednesday, July 18, 2007	Sheet 14 of 32



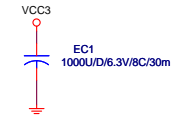
770-44-28SY00

U1E

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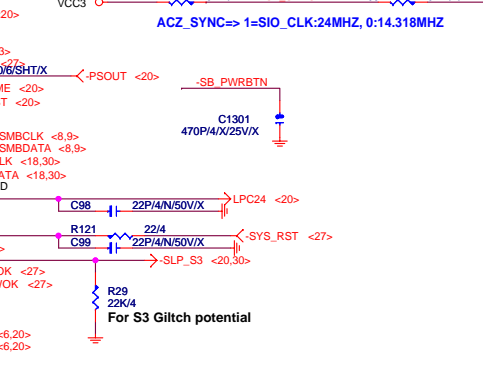
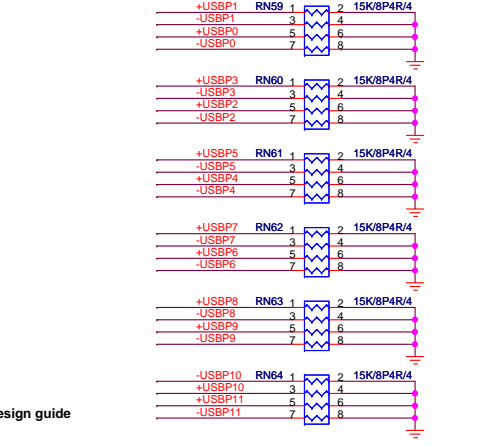
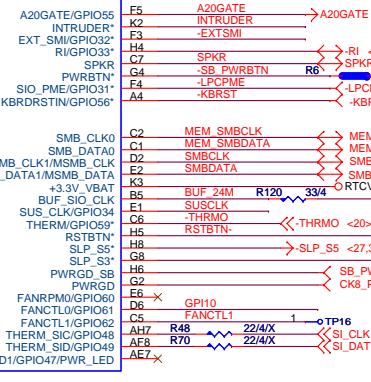
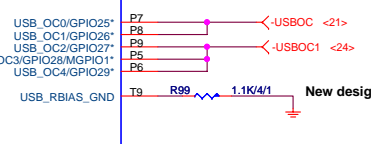
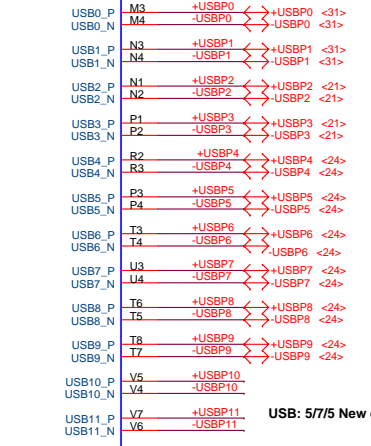
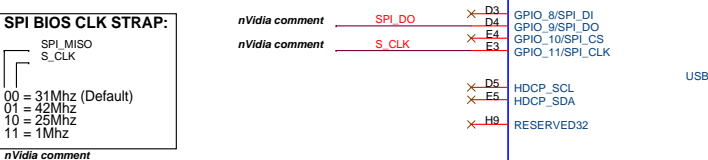
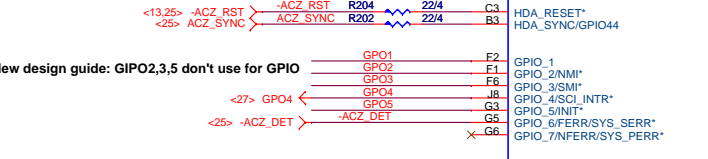
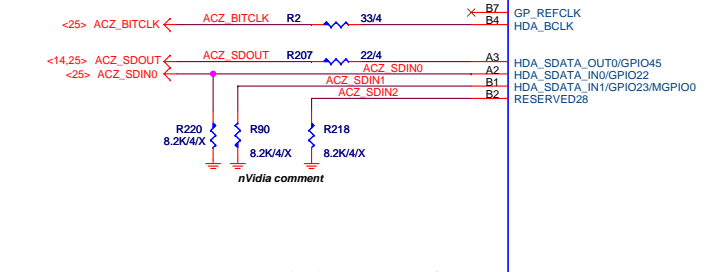


PCI LOADING

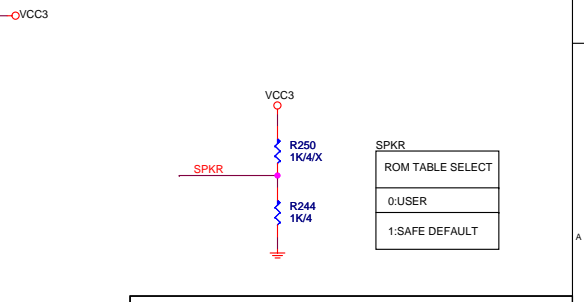
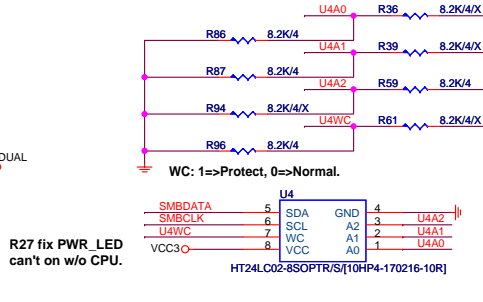
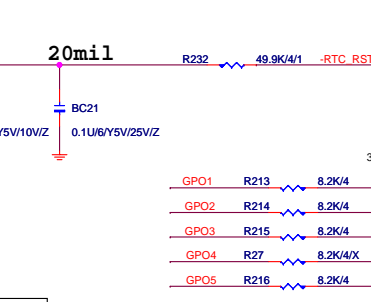
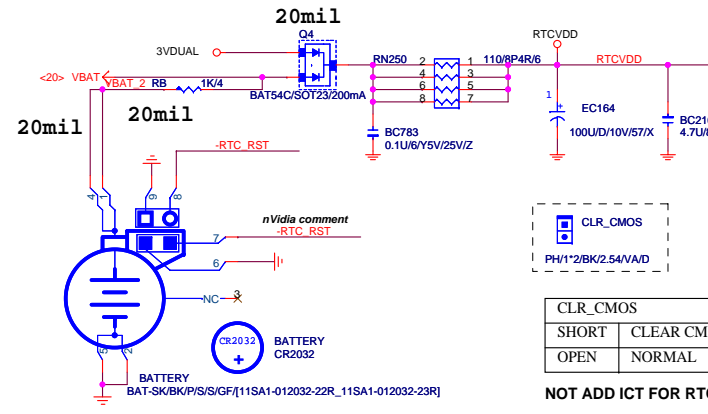
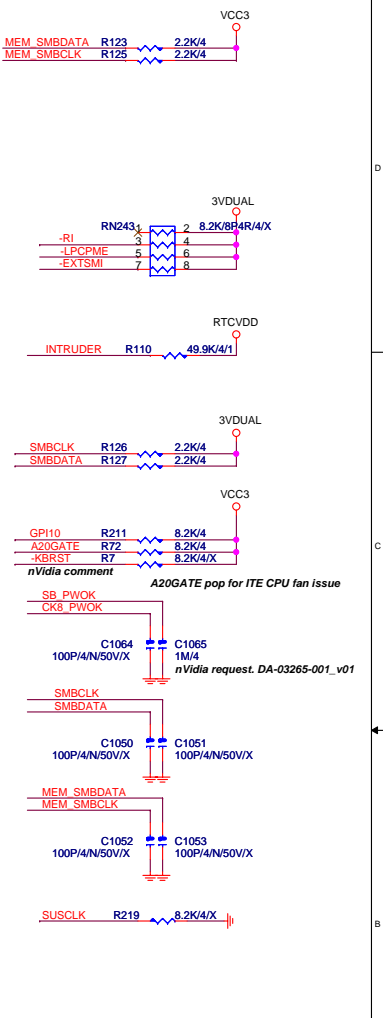


GIGABYTE		
MCP51-SATA IDE		
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		1.0

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C1065: Reference nVIDIA AP note DA-03265-001_v01



GIGABYTE

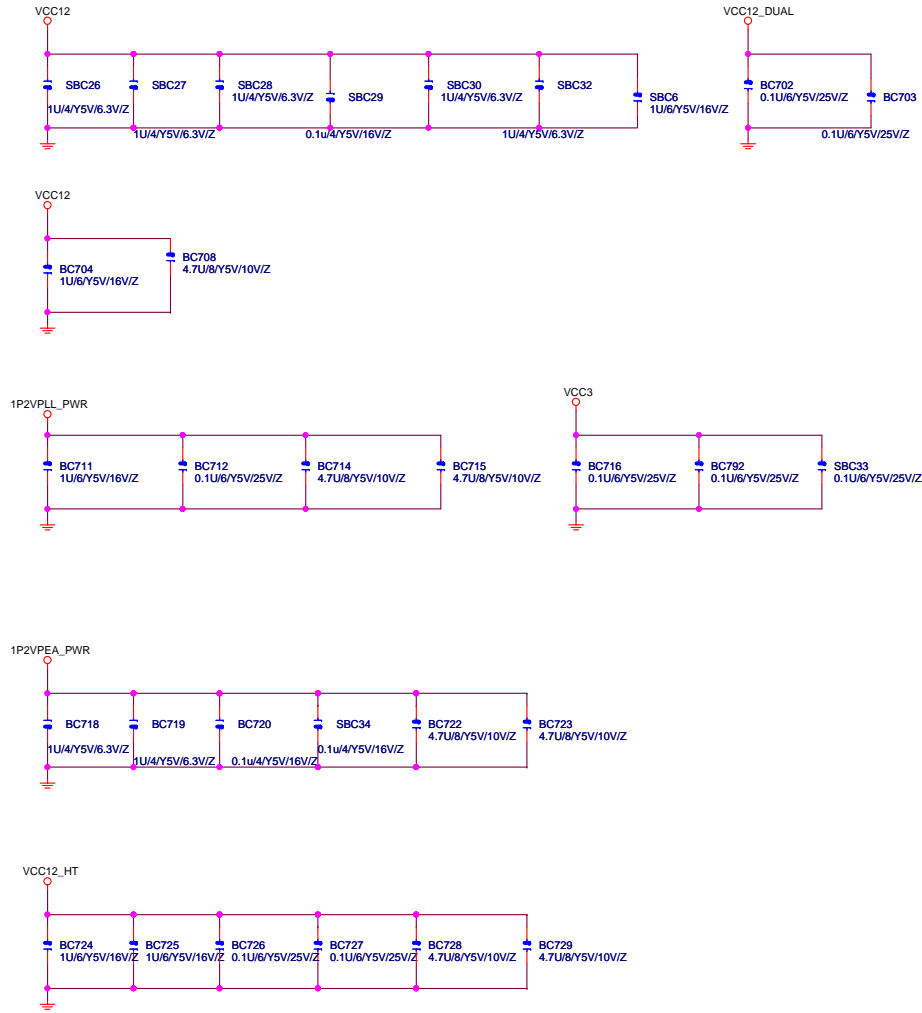
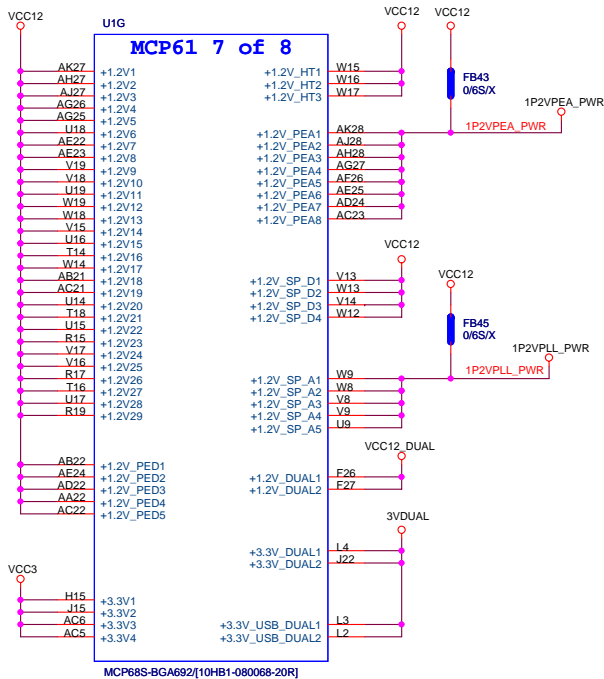
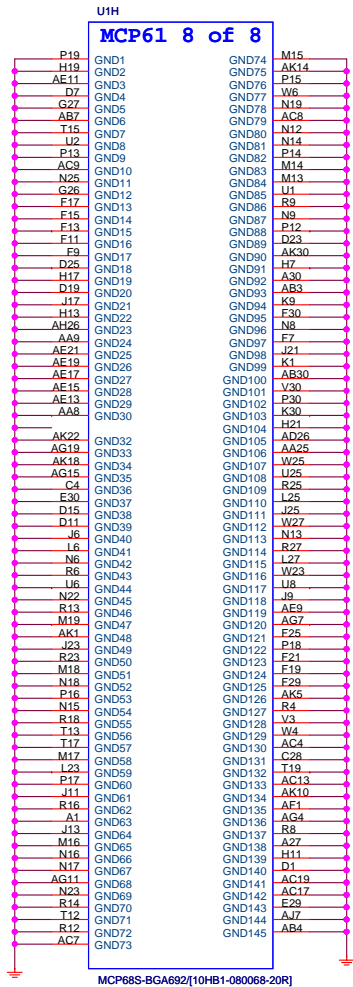
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Size: **GA-M68SM-S2** Rev: **1.0**

Document Number: **GA-M68SM-S2**

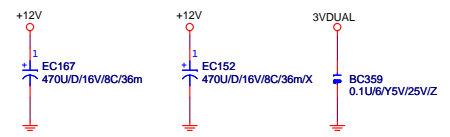
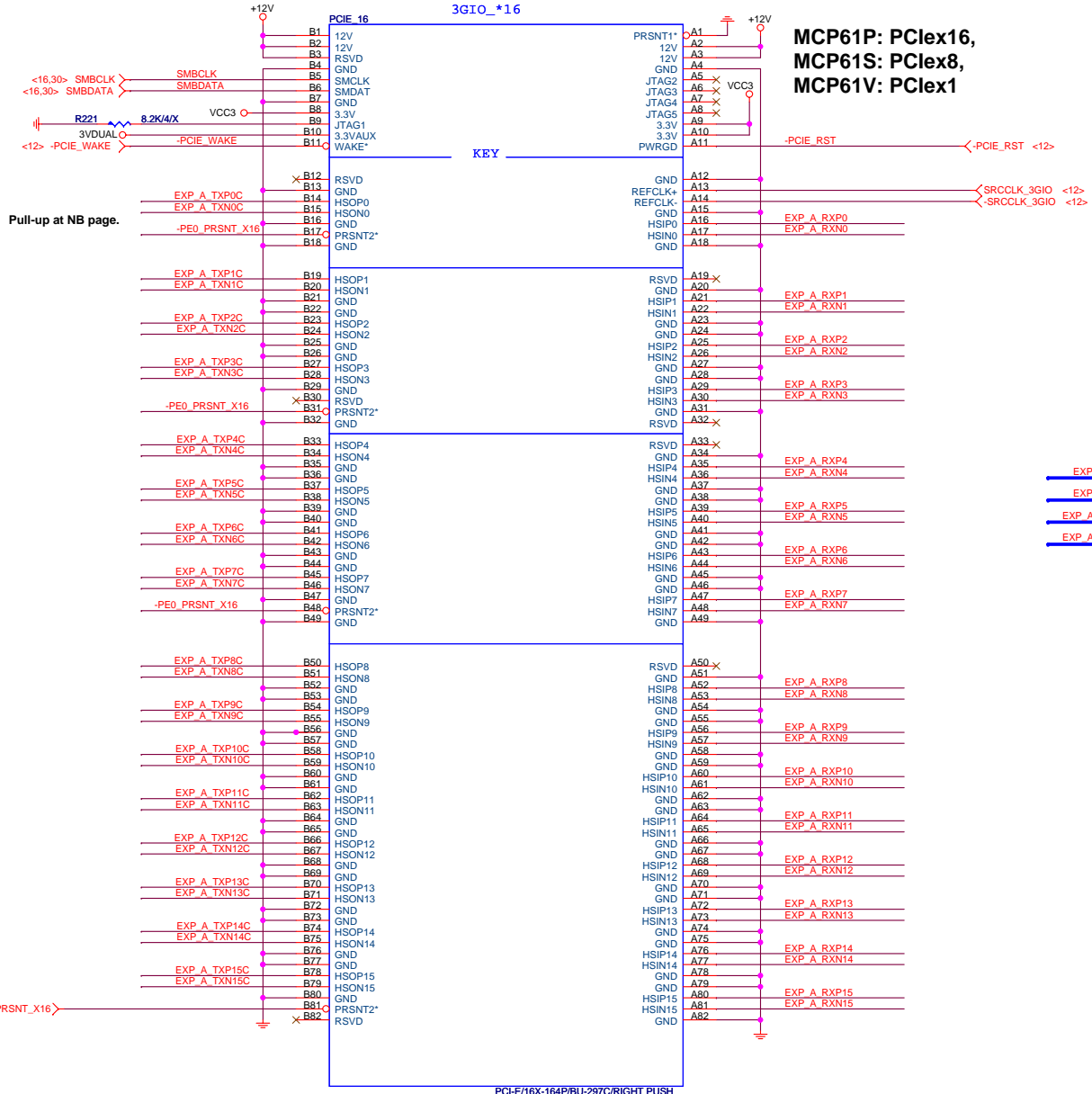
Date: Wednesday, July 18, 2007 Sheet 16 of 32

GPIO10,11:RSMRST*-->LOW
SO POWER PLUG,LOCKER NO CHANGE;
LOCKER MOVE BY TRIGGER(TEST
TIMING)

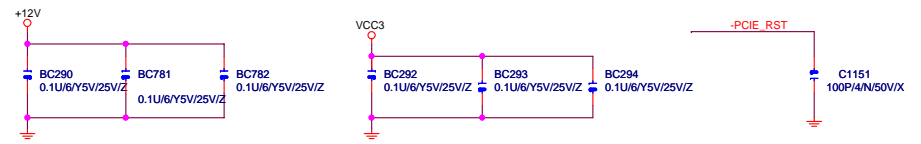
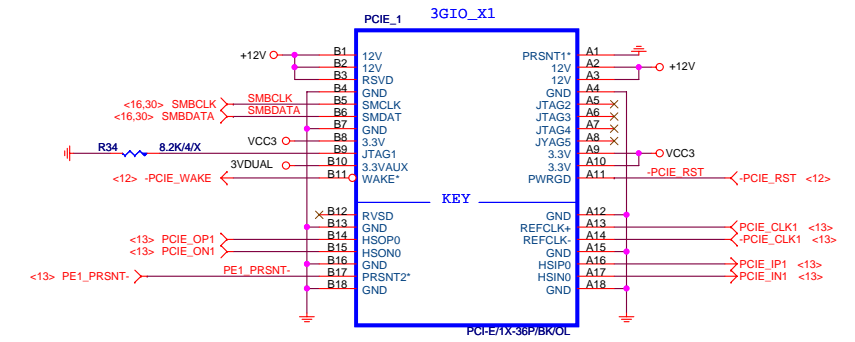
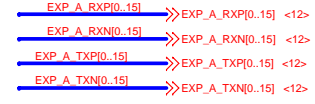


GIGABYTE		
MCP51-RGMII		
Title	Rev	
Document Number	1.0	
GA-M68SM-S2		
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**MCP61P: PCIe16,
MCP61S: PCIe8,
MCP61V: PCIe1**



EXP_A_TXP0	C127	0.1U/4/Y5V/16V/Z	EXP_A_TXP0C
EXP_A_TXN0	C128	0.1U/4/Y5V/16V/Z	EXP_A_TXN0C
EXP_A_TXP1	C129	0.1U/4/Y5V/16V/Z	EXP_A_TXP1C
EXP_A_TXN1	C130	0.1U/4/Y5V/16V/Z	EXP_A_TXN1C
EXP_A_TXP2	C131	0.1U/4/Y5V/16V/Z	EXP_A_TXP2C
EXP_A_TXN2	C132	0.1U/4/Y5V/16V/Z	EXP_A_TXN2C
EXP_A_TXP3	C133	0.1U/4/Y5V/16V/Z	EXP_A_TXP3C
EXP_A_TXN3	C134	0.1U/4/Y5V/16V/Z	EXP_A_TXN3C
EXP_A_TXP4	C135	0.1U/4/Y5V/16V/Z	EXP_A_TXP4C
EXP_A_TXN4	C136	0.1U/4/Y5V/16V/Z	EXP_A_TXN4C
EXP_A_TXP5	C137	0.1U/4/Y5V/16V/Z	EXP_A_TXP5C
EXP_A_TXN5	C138	0.1U/4/Y5V/16V/Z	EXP_A_TXN5C
EXP_A_TXP6	C139	0.1U/4/Y5V/16V/Z	EXP_A_TXP6C
EXP_A_TXN6	C140	0.1U/4/Y5V/16V/Z	EXP_A_TXN6C
EXP_A_TXP7	C141	0.1U/4/Y5V/16V/Z	EXP_A_TXP7C
EXP_A_TXN7	C142	0.1U/4/Y5V/16V/Z	EXP_A_TXN7C
EXP_A_TXP8	C143	0.1U/4/Y5V/16V/Z	EXP_A_TXP8C
EXP_A_TXN8	C144	0.1U/4/Y5V/16V/Z	EXP_A_TXN8C
EXP_A_TXP9	C145	0.1U/4/Y5V/16V/Z	EXP_A_TXP9C
EXP_A_TXN9	C146	0.1U/4/Y5V/16V/Z	EXP_A_TXN9C
EXP_A_TXP10	C147	0.1U/4/Y5V/16V/Z	EXP_A_TXP10C
EXP_A_TXN10	C148	0.1U/4/Y5V/16V/Z	EXP_A_TXN10C
EXP_A_TXP11	C149	0.1U/4/Y5V/16V/Z	EXP_A_TXP11C
EXP_A_TXN11	C150	0.1U/4/Y5V/16V/Z	EXP_A_TXN11C
EXP_A_TXP12	C151	0.1U/4/Y5V/16V/Z	EXP_A_TXP12C
EXP_A_TXN12	C153	0.1U/4/Y5V/16V/Z	EXP_A_TXN12C
EXP_A_TXP13	C155	0.1U/4/Y5V/16V/Z	EXP_A_TXP13C
EXP_A_TXN13	C156	0.1U/4/Y5V/16V/Z	EXP_A_TXN13C
EXP_A_TXP14	C157	0.1U/4/Y5V/16V/Z	EXP_A_TXP14C
EXP_A_TXN14	C158	0.1U/4/Y5V/16V/Z	EXP_A_TXN14C
EXP_A_TXP15	C159	0.1U/4/Y5V/16V/Z	EXP_A_TXP15C
EXP_A_TXN15	C160	0.1U/4/Y5V/16V/Z	EXP_A_TXN15C



GIGABYTE

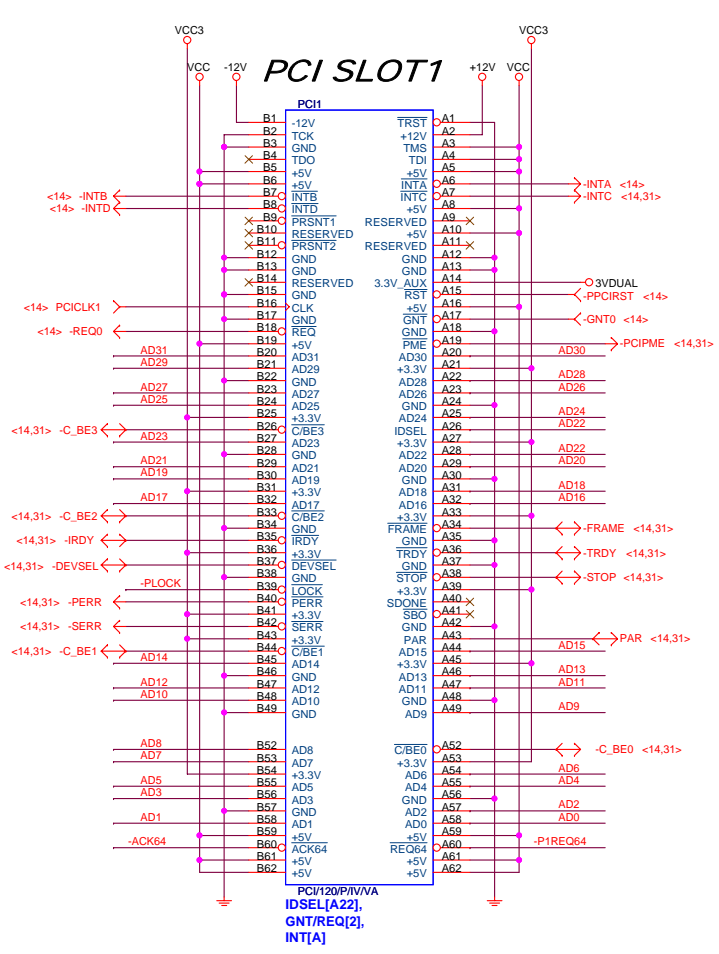
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Document Number: **GA-M68SM-S2**

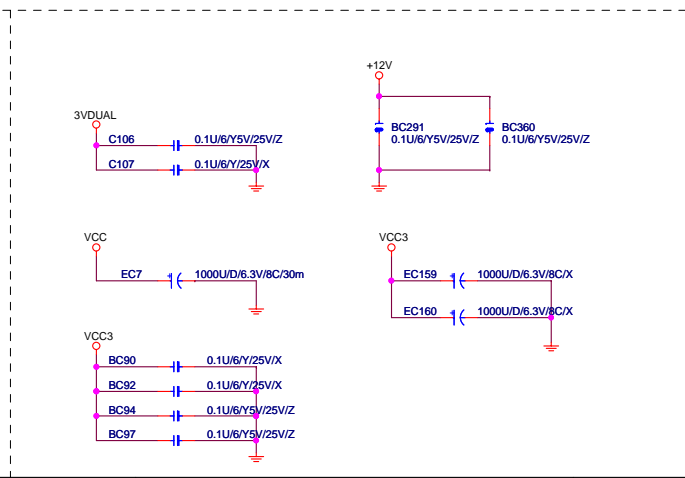
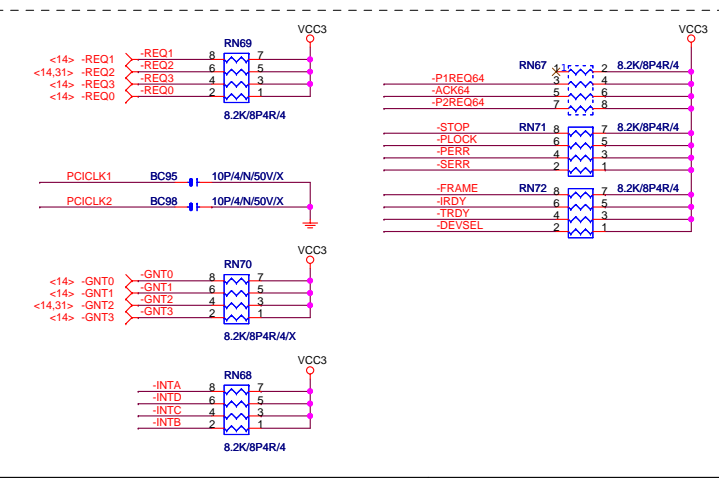
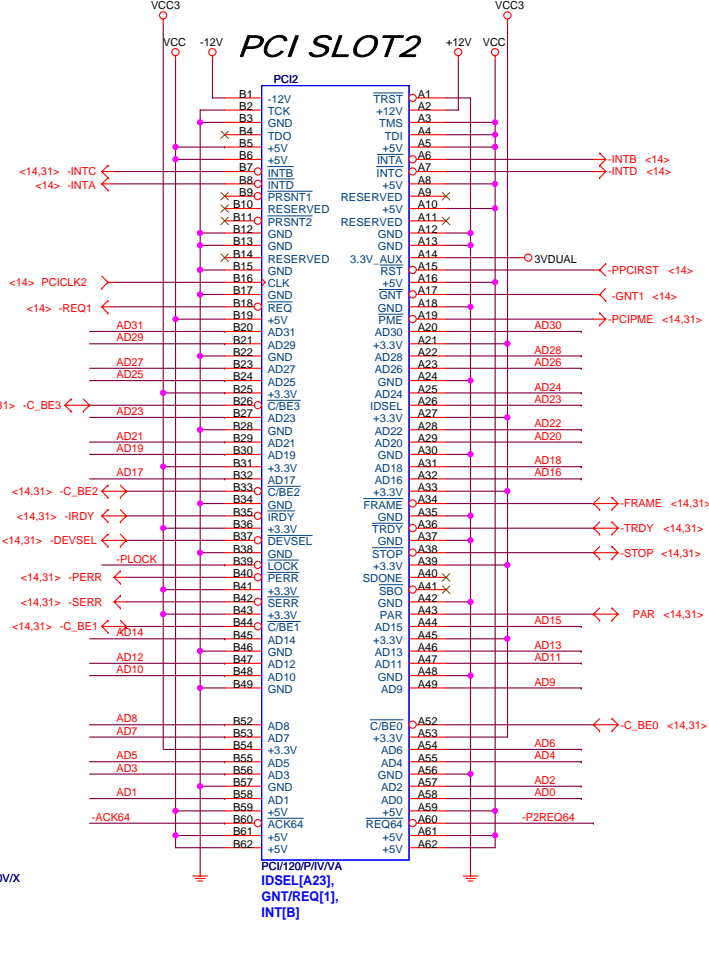
Rev: **1.0**

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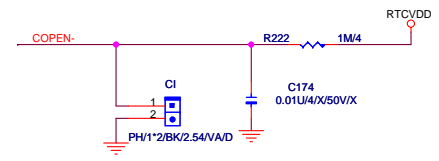
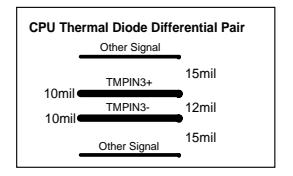
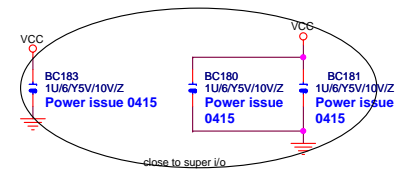
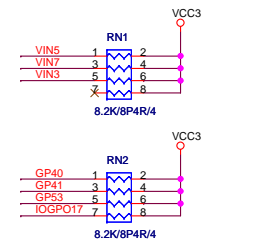
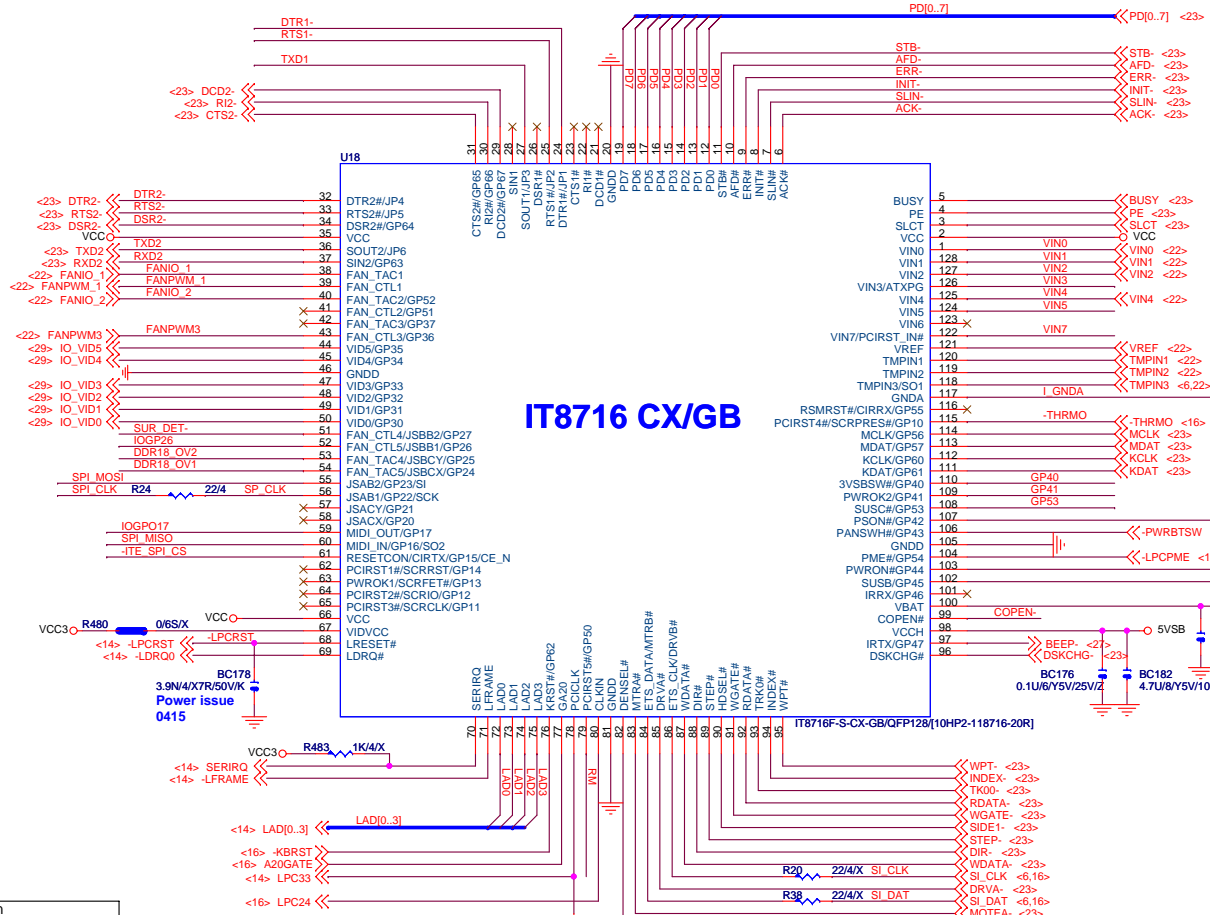
PCI SLOT 1,2,3



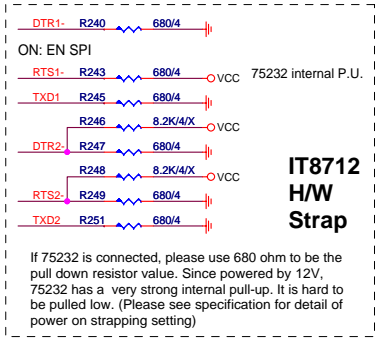
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GIGABYTE		
PCI SLOT 1,2,3		
Title	Document Number	Rev
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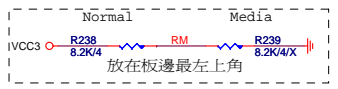
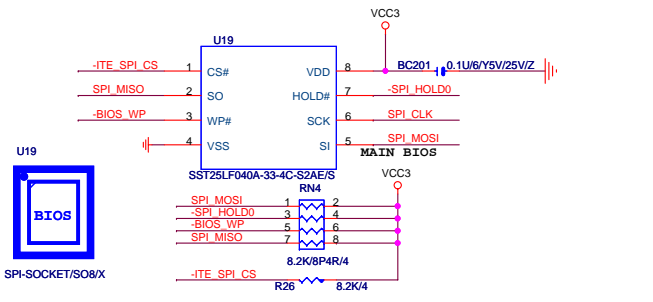


Default	Description
DTR1- 0	En SPI Flash
RTS1- 1	Midi-in/SO2 as SPI SO pin
TXD1- --	
DTR2- 0	PCIRSTx# are push-pull
RTS2- 0	Power-on FAN Duty=50%
TXD2- 0	VID threshold is 0.8V/0.4V



IT8712 H/W Strap

If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)



Power On Strapping Options

Symbol	value	Description
JP1	Flashseg1_EN	0 Disabled. 1 Flash I/F Address Segment 1 (FFF8_0000h-FFFF_FFFFh, 000E_0000h-000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1 FLH_SO2 is selected as the Serial Flash I/F SO pin. 0 FLH_S01 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	-- Chip selection in configuration.
JP4	BUF_SEL	1 The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10-20 ns when the signal transits from low to high, and then Hi-Z. 0 The output buffers are push-pull.
JP5	FAN_CTL_SEL	1 The default value of EC Index 15h / 16h / 17h is 00h 0 The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1 The threshold voltage of VID is 2.0 / 0.8V 0 The threshold voltage of VID is 0.8 / 0.4V

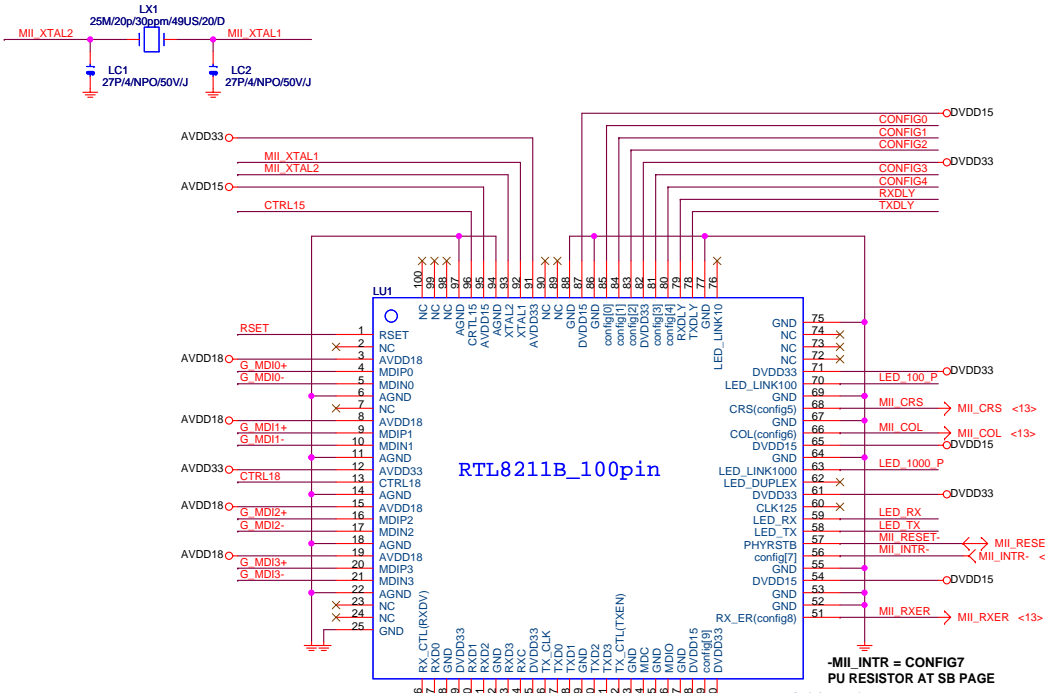
GIGABYTE

Title: **ITE 8712 LPC IO**

Size: **GA-M6SM-S2**

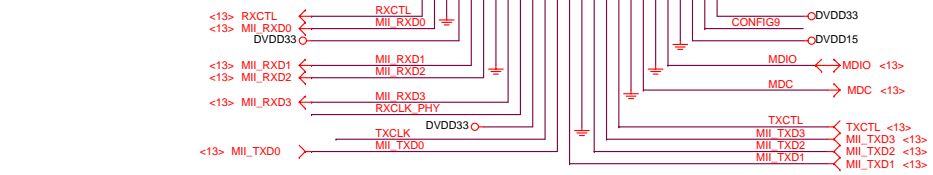
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Rev: **1.0**



RTL8211B_100pin

-MII_INTR = CONFIG7
PU RESISTOR AT SB PAGE



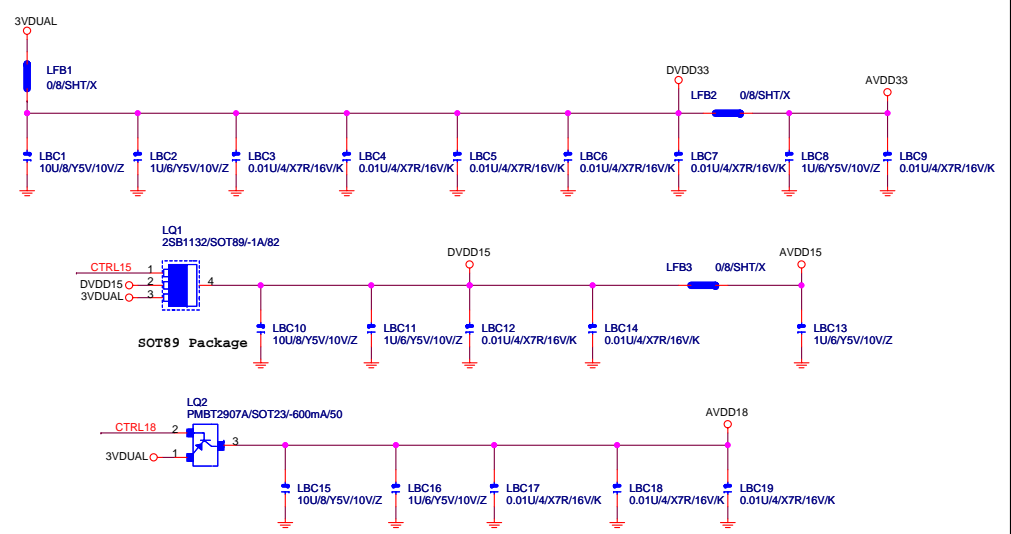
For latching 1000MB timing: 4/18



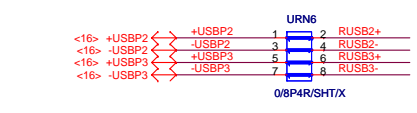
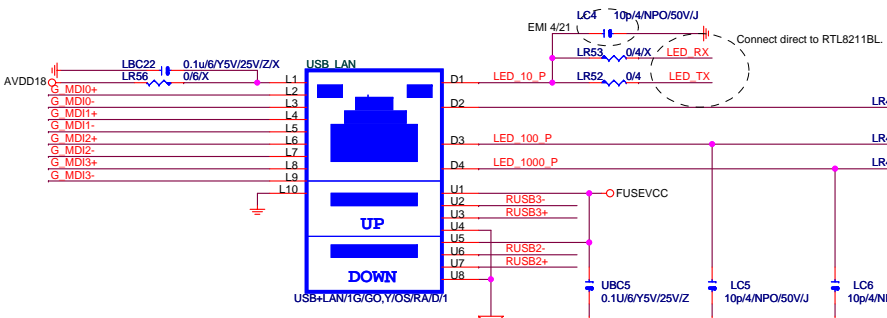
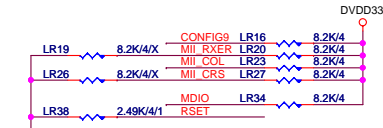
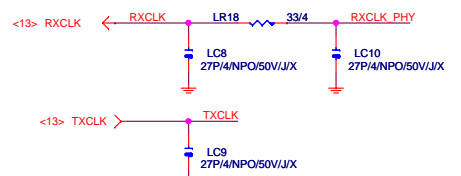
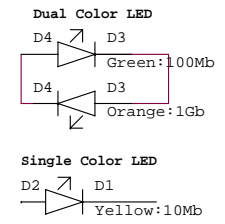
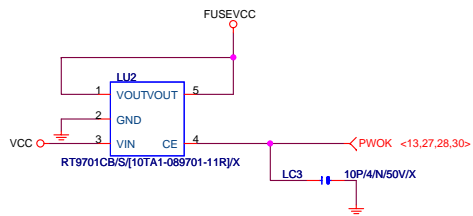
TXDLY/RXDLY IS FOR RTL8211BL RGMII USE
WITHOUT TX/RX DELAY: PU REMOVED
RTL8201: TXDLY/RXDLY ALL ARE NC

- 1.RTL8211BL: H/W CONFIG 1111-nWAY, ADVERTISE ALL CAPABILITIES, PREFER SLAVE CRS PU REMOVED
- 2.RTL8201: CONFIG7,9, RX_ER, CRS PU REMOVED
- REST:
RTL8201BC: 5.9K
RTL8201CL/CP: 2K
RTL8211BL: 2.49K

- 1.RTL8211BL: H/W CONFIG43210=00001,
2.RTL8201: CONFIG43210 --> NC

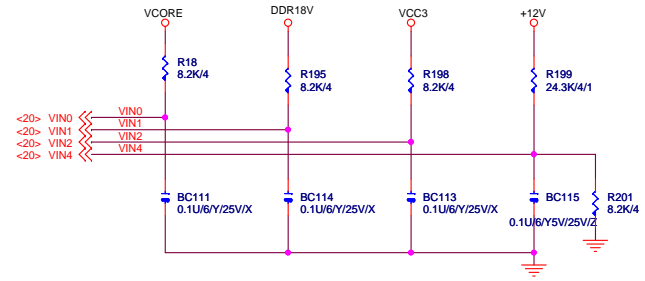
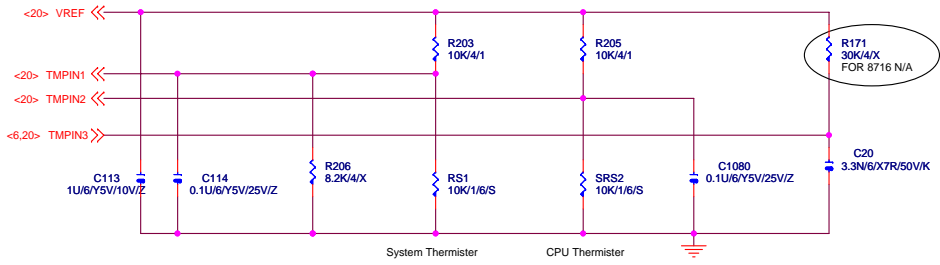


- 1.RTL8211BL: H/W CONFIG43210=00001,
2.RTL8201: CONFIG43210 --> NC

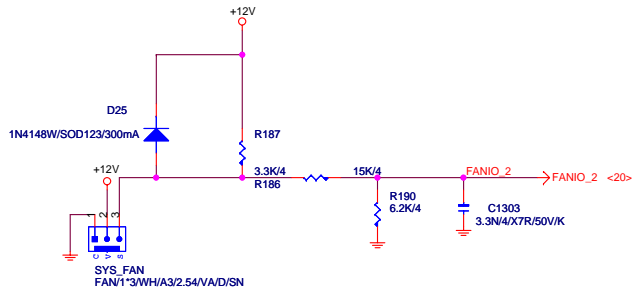


GIGABYTE			
Realtek 8211b			
Title	Document Number	Rev	
	GA-M68SM-S2	1.0	
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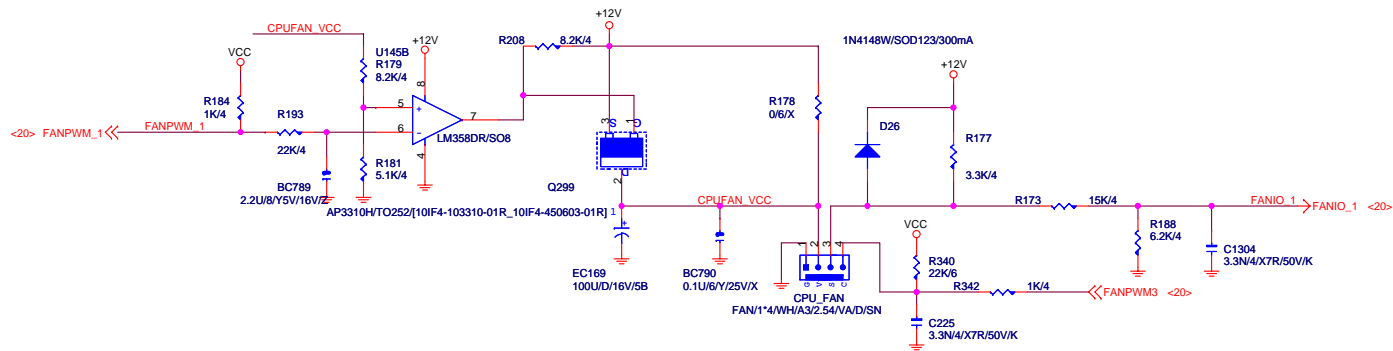
Hardware Monitor circuits



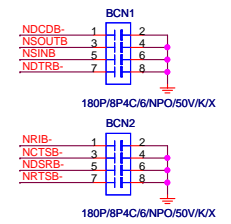
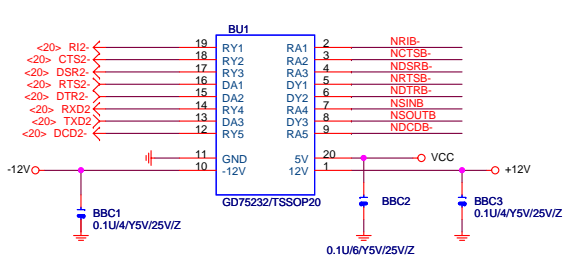
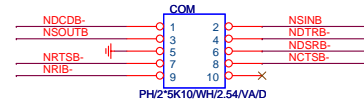
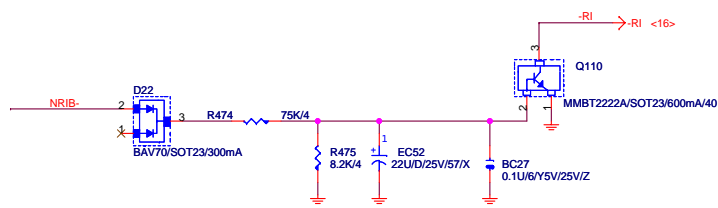
SYSTEM FAN



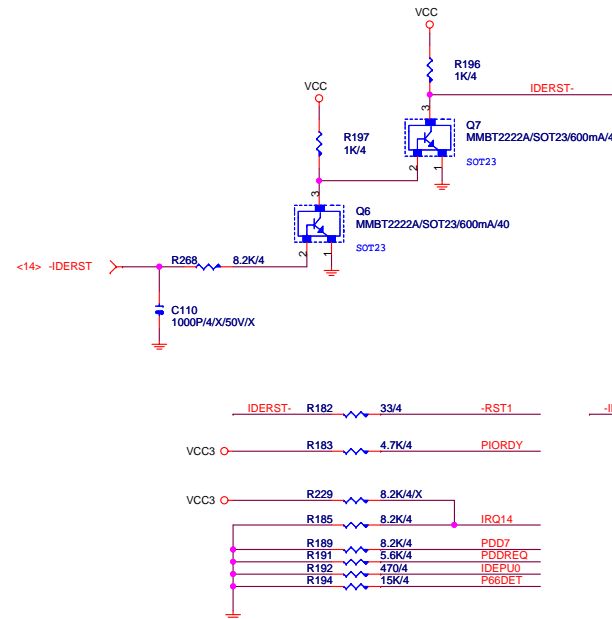
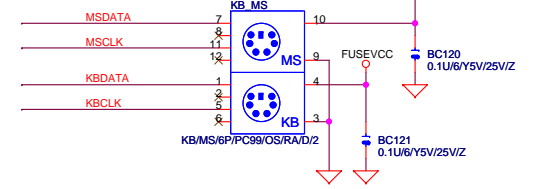
CPU FAN



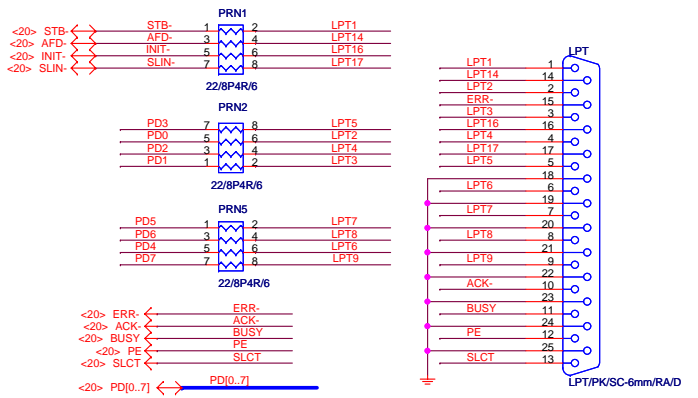
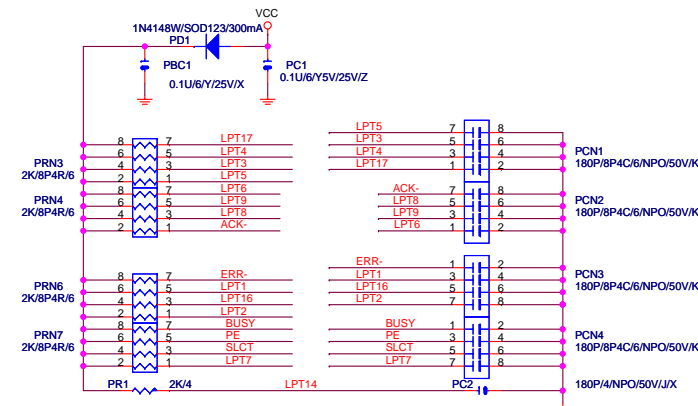
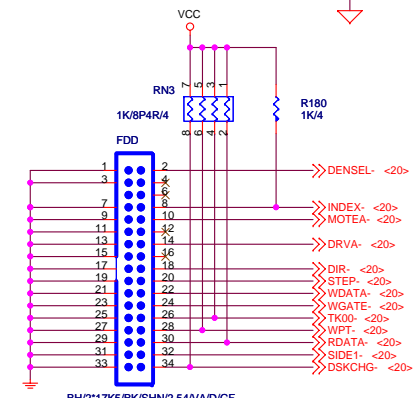
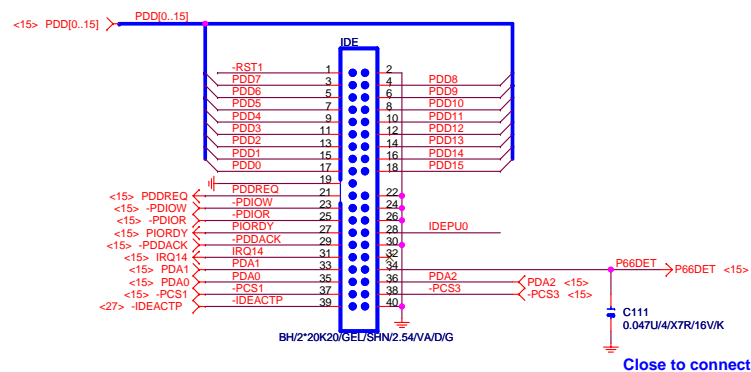
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Title	FANHWMO	
Size	Document Number	Rev
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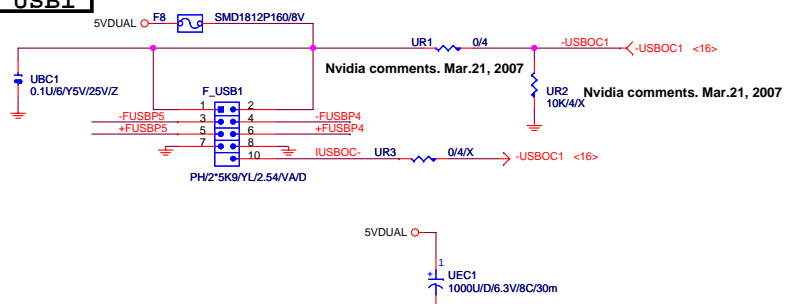
KB & MS



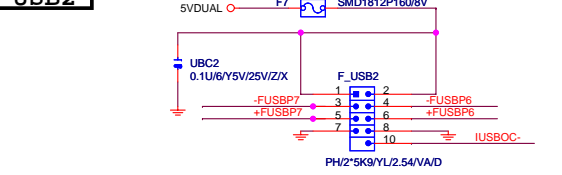
PRIMARY IDE CONNECTOR



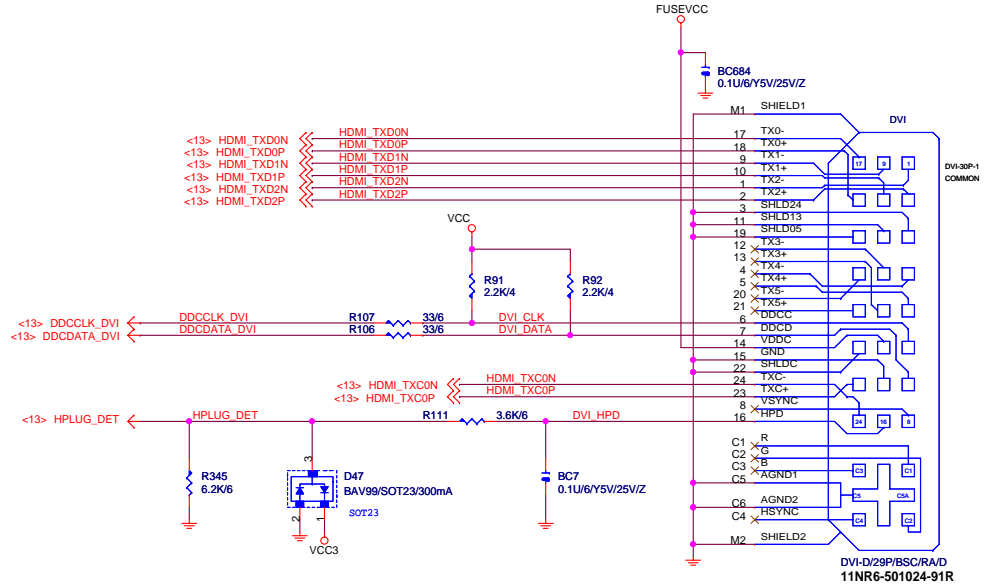
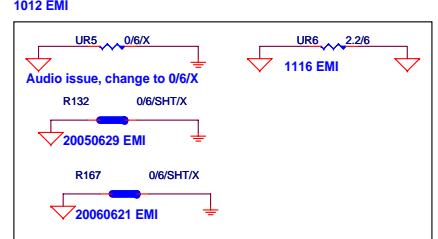
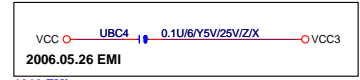
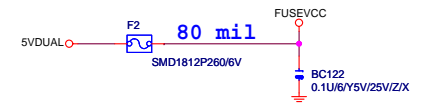
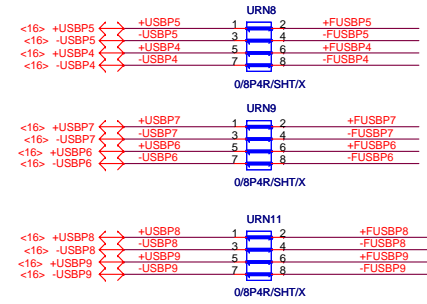
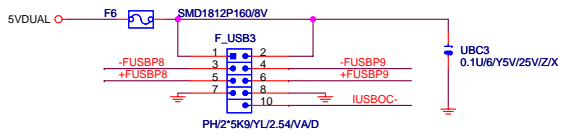
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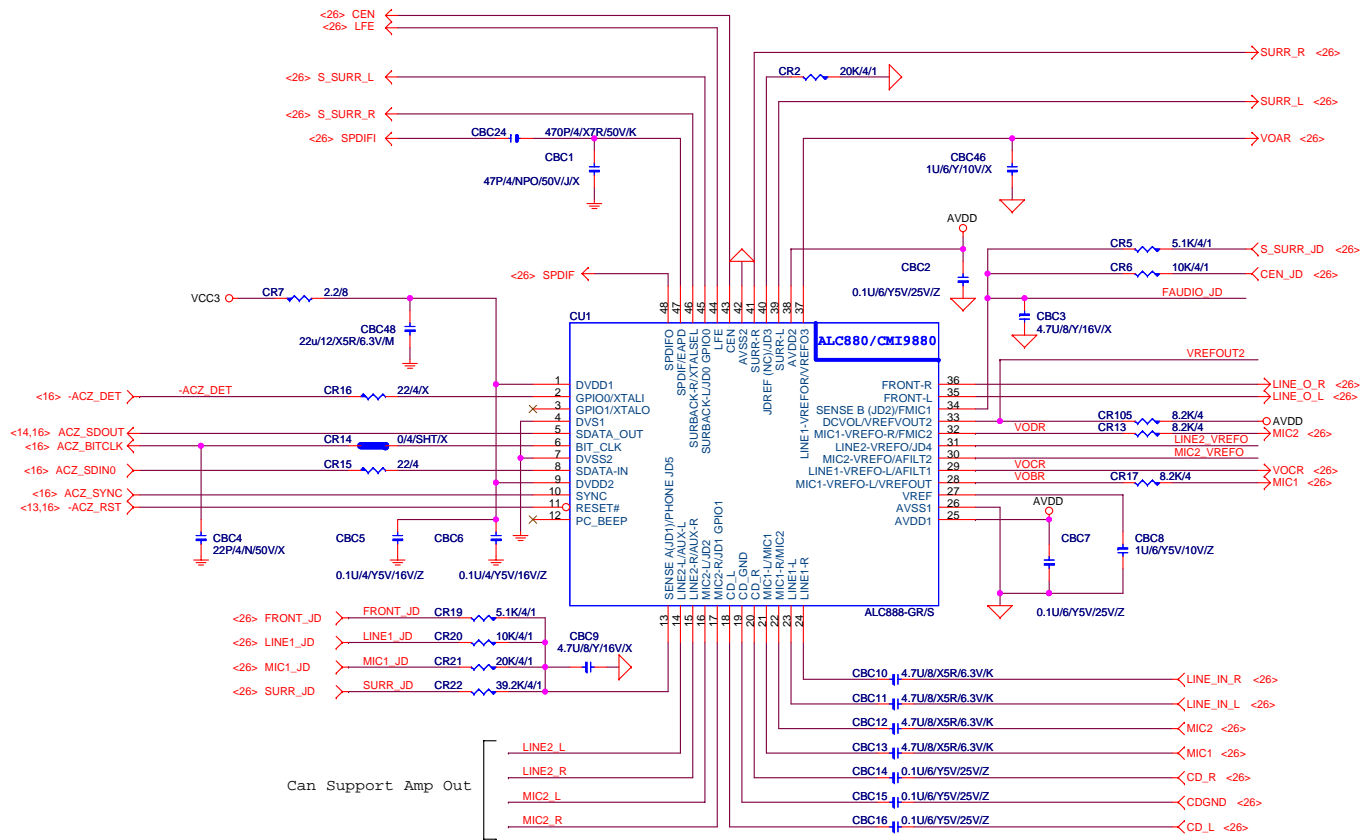
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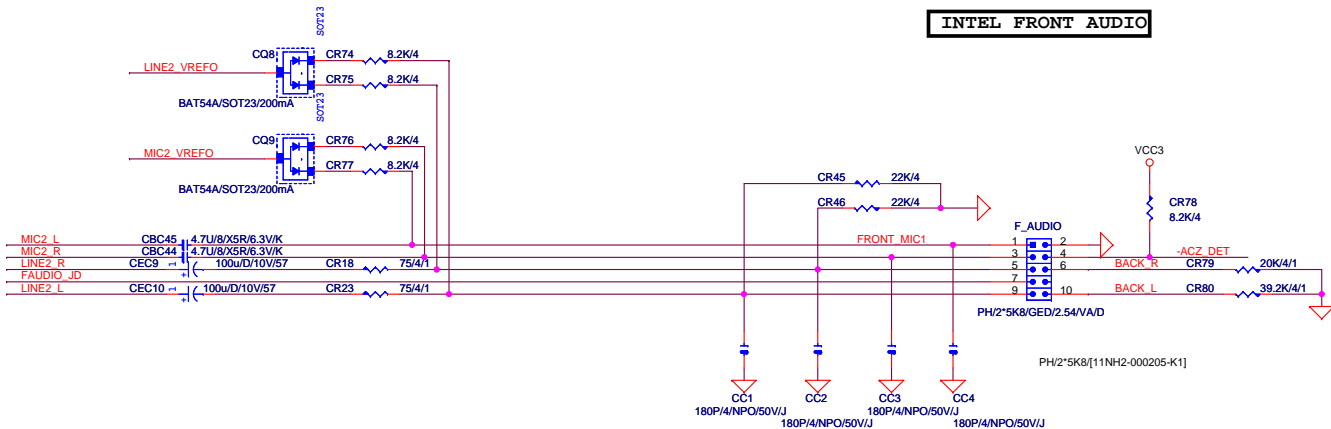
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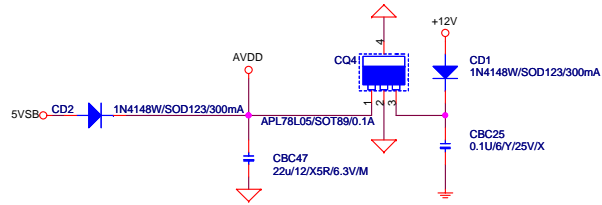
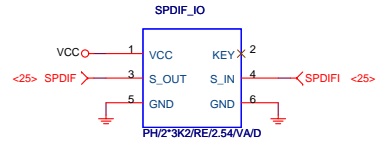
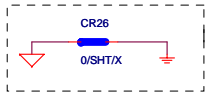
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Title	Document Number	Rev	
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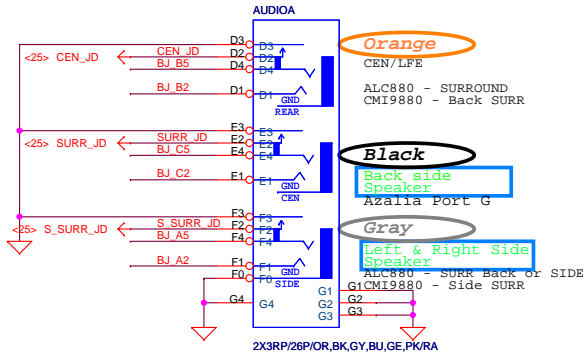
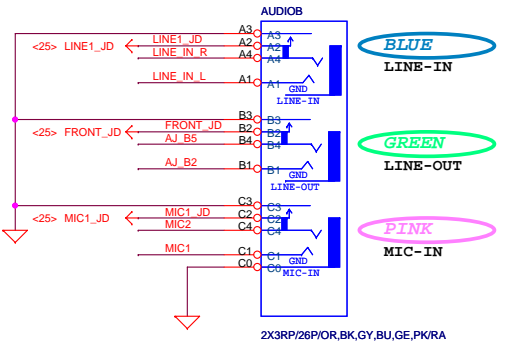
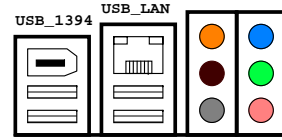
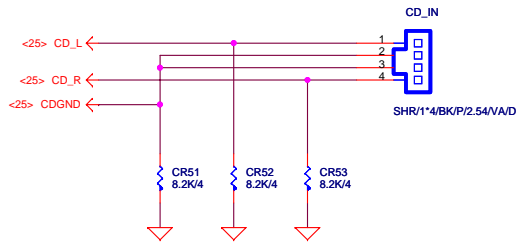
INTEL FRONT AUDIO



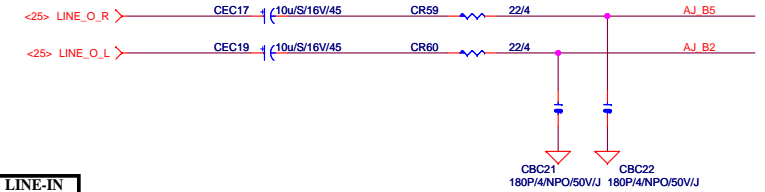
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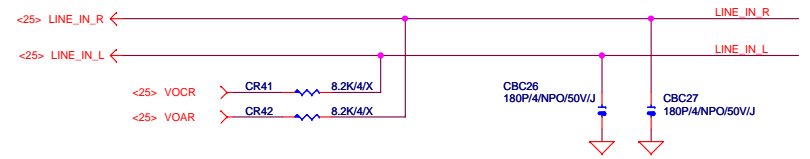
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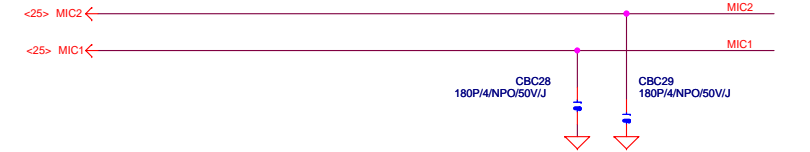
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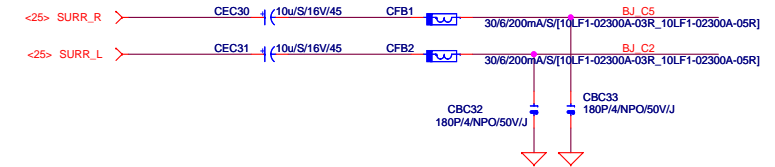
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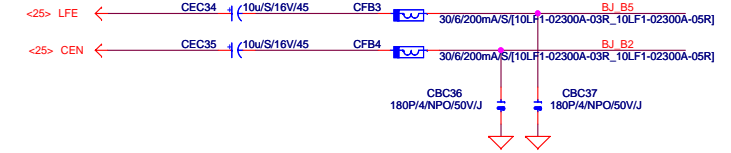
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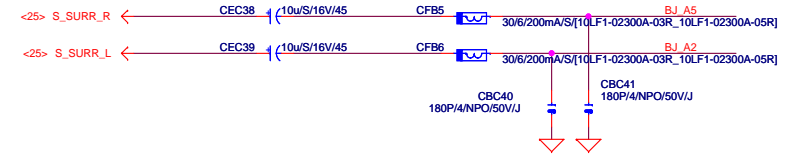
SURROUND



CEN/LFE

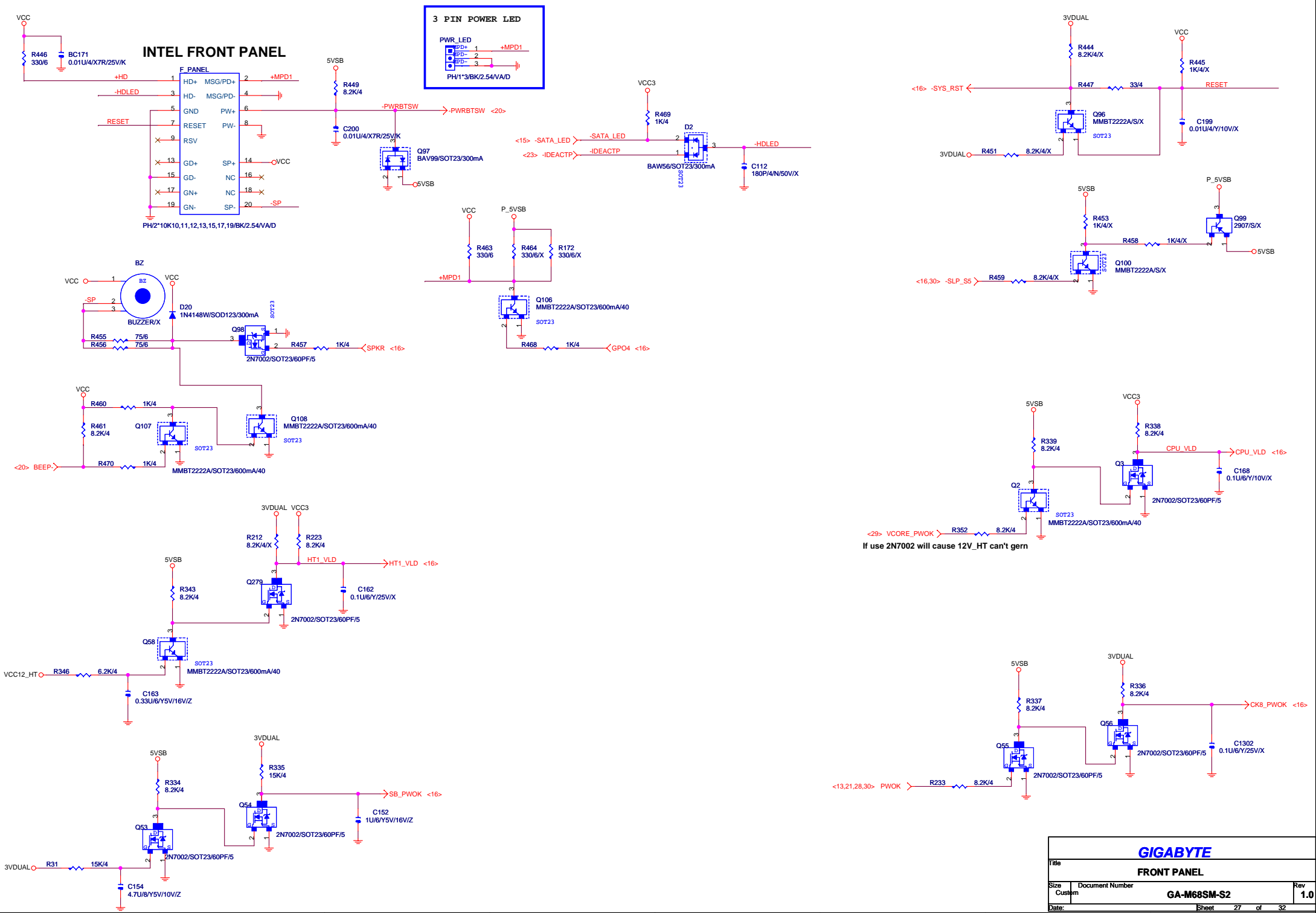
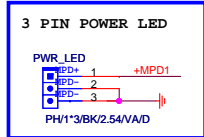


SURR BACK



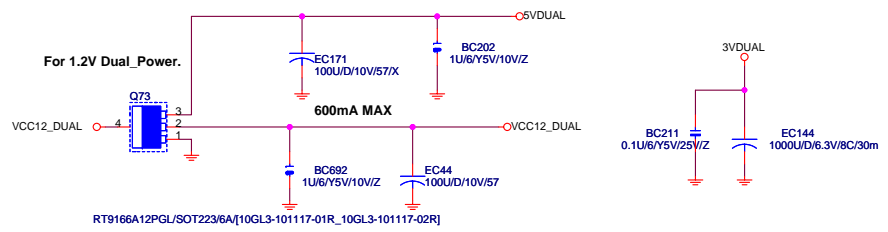
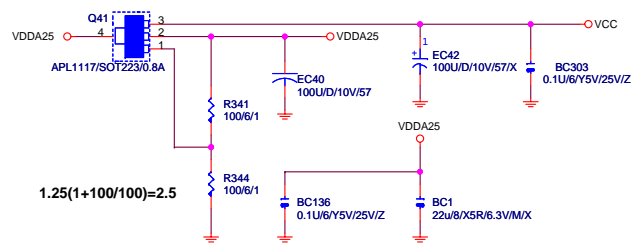
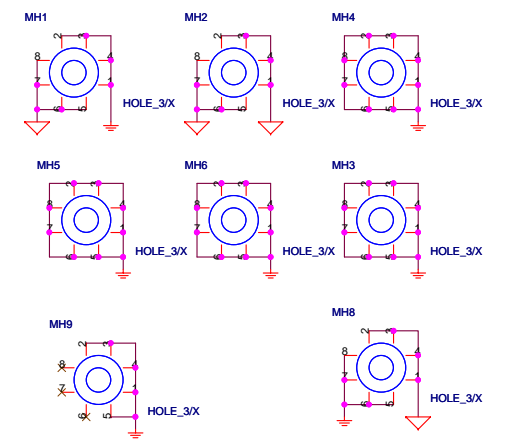
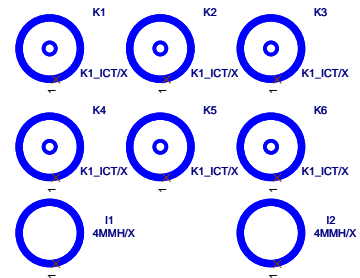
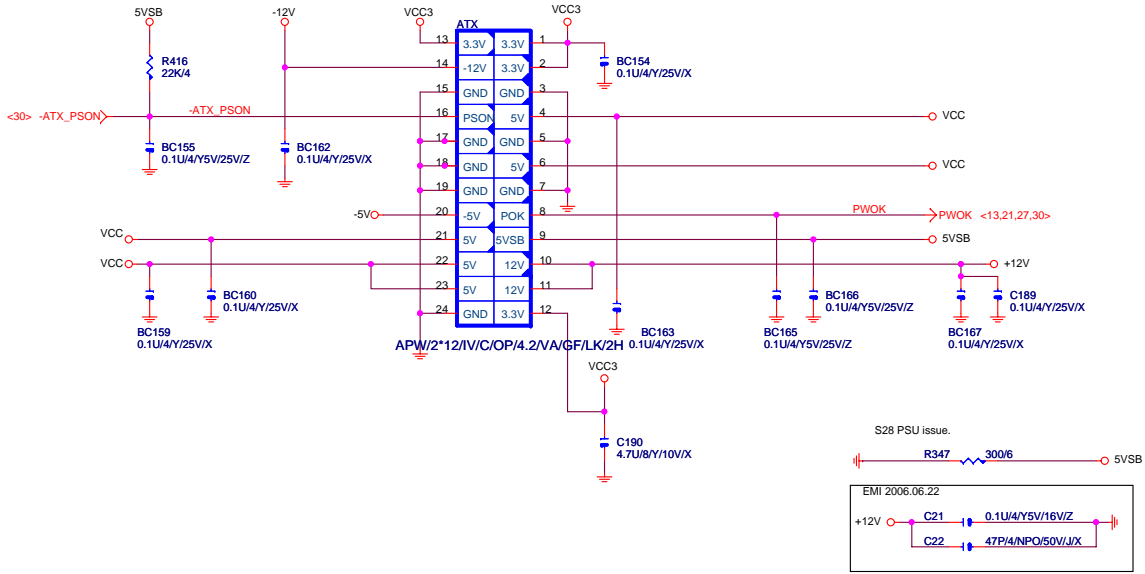
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Size	Document Number	Rev
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INTEL FRONT PANEL

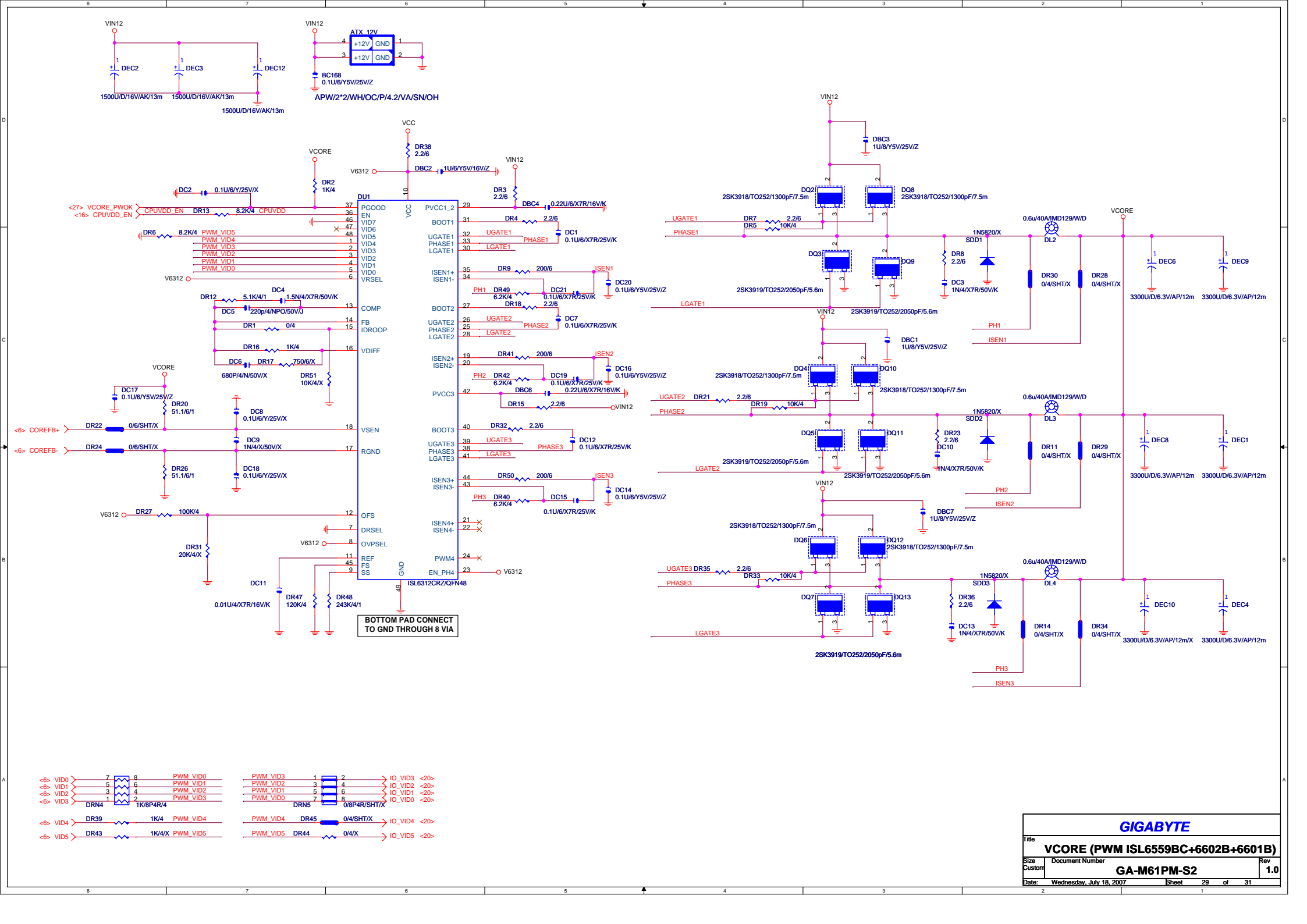


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Title	Document Number	Rev
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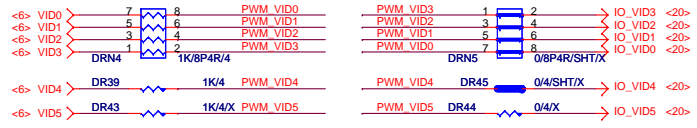
ATX POWER CONNECTOR



GIGABYTE		
Title	Misc. PWR & ATX CONN	
Size	Document Number	Rev
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BOTTOM PAD CONNECT TO GND THROUGH 8 VIA



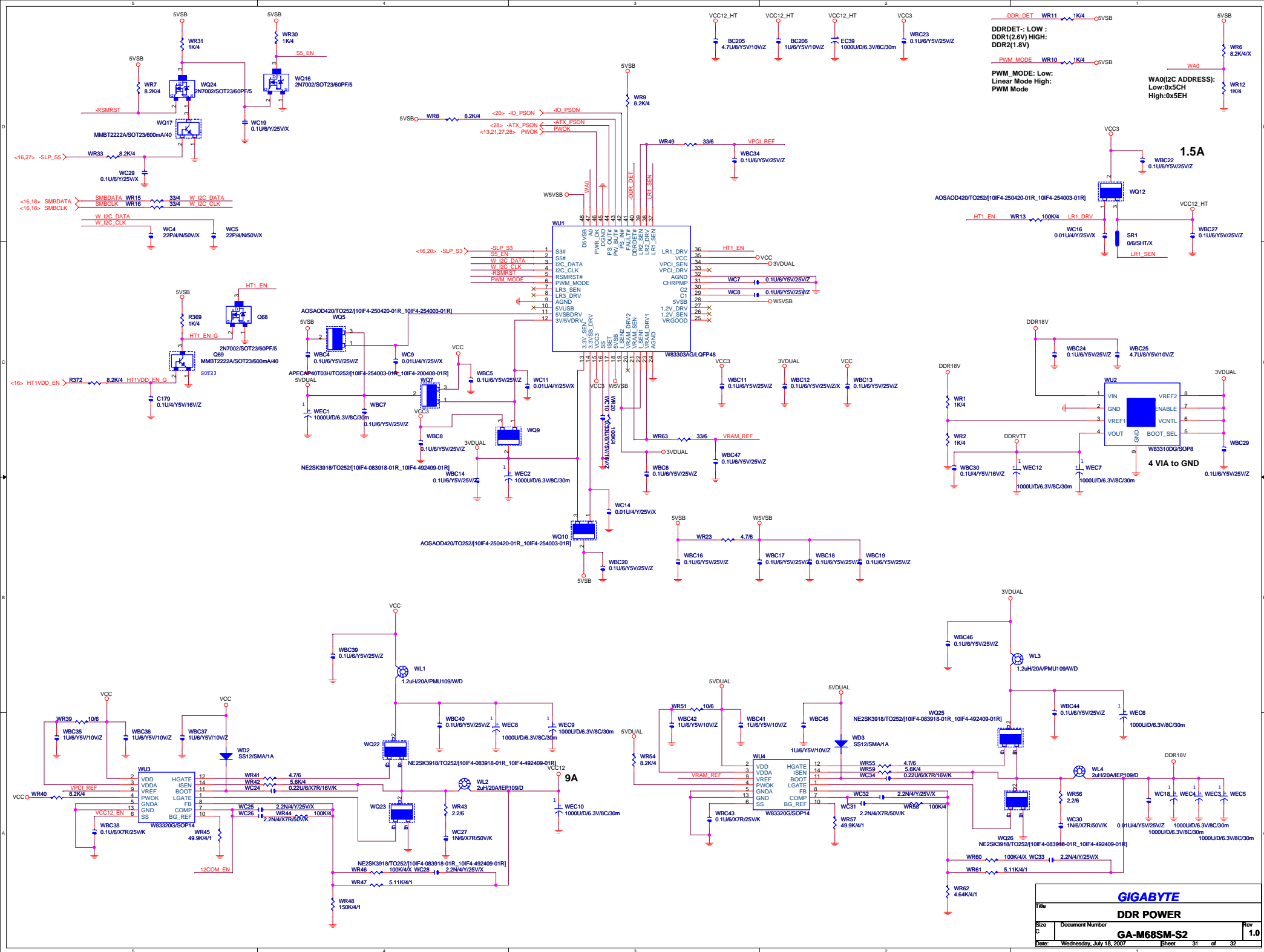
GIGABYTE

Title: **VCORE (PWM ISL6559BC+6602B+6601B)**

Size: Document Number

Custom: **GA-M61PM-S2** Rev: **1.0**

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DDRDET-: LOW :
DDR1(2.6V) HIGH:
DDR2(1.8V)

PWM_MODE WR10 1K/4 C5V5B

PWM Mode:
 Linear Mode High:
 PWM Mode

WA0(I2C ADDRESS):
 Low:0x5CH
 High:0x5EH

